Design Rule Verification Report

Date:	11/12/2019	**Warnings:**	0
Time:	4:00:35 PM	**Rule Violations:**	0
Elapsed Time:	00:00:00	**Waived Violations:**	24
Filename:	C:\Users\mmatusek\Documents\Altium Projects\ELEG_312_FP\Filter.PcbDoc		

Summary

Warnings	**Count**
Total	**0**

Rule Violations	**Count**
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=52.323mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4) (All)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	0
Silk to Silk (Clearance=10mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Room Filter (Bounding Region = (11713.739mil, 6581.063mil, 15191.929mil, 10381.416mil) (InComponentClass('Filter'))	0

Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	**0**

Waived Violations	**Count**
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	3
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	19
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	2
Total	**24**

Rule Violations

Waived Violations

Minimum Solder Mask Sliver (Gap=10mil) (All),(All)

Minimum Solder Mask Sliver Constraint: (9.718mil < 10mil) Between Pad C10-1(2160mil,1612.912mil) on Top Layer And Pad C10-2(2160mil,1670mil) on Top Layer [Top Solder] Mask Sliver [9.718mil]
Waived by Matthew Matusek at 11/7/2019 4:12:13 PM

Minimum Solder Mask Sliver Constraint: (9.718mil < 10mil) Between Pad C7-1(2270mil,498.544mil) on Top Layer And Pad C7-2(2270mil,441.456mil) on Top Layer [Top Solder] Mask Sliver [9.718mil]
Waived by Matthew Matusek at 11/7/2019 4:12:37 PM

Minimum Solder Mask Sliver Constraint: (9.718mil < 10mil) Between Pad C8-1(3150mil,2780mil) on Top Layer And Pad C8-2(3207.088mil,2780mil) on Top Layer [Top Solder] Mask Sliver [9.718mil]
Waived by Matthew Matusek at 11/7/2019 4:12:29 PM

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Silk To Solder Mask (Clearance=10mil) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (9.719mil < 10mil) Between Pad C6-2(1540mil,502.5mil) on Multi-Layer And Text "C6" (1510mil,540mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.719mil]
Waived by Matthew Matusek at 11/7/2019 4:14:31 PM

Silk To Solder Mask Clearance Constraint: (9.929mil < 10mil) Between Pad S1-1(200mil,2680mil) on Multi-Layer And Track (70.078mil,2744.96mil)(520.078mil,2744.96mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.929mil]
Waived by Matthew Matusek at 11/7/2019 4:18:18 PM

Silk To Solder Mask Clearance Constraint: (9.238mil < 10mil) Between Pad S1-3(200mil,2309.922mil) on Multi-Layer And Track (70.078mil,2244.96mil)(520.078mil,2244.96mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.238mil]
Waived by Matthew Matusek at 11/7/2019 4:15:22 PM

Silk To Solder Mask Clearance Constraint: (9.238mil < 10mil) Between Pad S1-4(390.158mil,2309.922mil) on Multi-Layer And Track (70.078mil,2244.96mil)(520.078mil,2244.96mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.238mil]
Waived by Matthew Matusek at 11/7/2019 4:15:28 PM

Silk To Solder Mask Clearance Constraint: (9.929mil < 10mil) Between Pad S1-6(390.158mil,2680mil) on Multi-Layer And Track (70.078mil,2744.96mil)(520.078mil,2744.96mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.929mil]
Waived by Matthew Matusek at 11/7/2019 4:14:48 PM

Silk To Solder Mask Clearance Constraint: (9.236mil < 10mil) Between Pad S2-1(1700mil,2564.96mil) on Multi-Layer And Track (1564.96mil,2500mil)(1835.04mil,2500mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.236mil]
Waived by Matthew Matusek at 11/7/2019 4:15:46 PM

Silk To Solder Mask Clearance Constraint: (9.929mil < 10mil) Between Pad S2-3(1700mil,2935.04mil) on Multi-Layer And Track (1564.96mil,3000mil)(1835.04mil,3000mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.929mil]
Waived by Matthew Matusek at 11/7/2019 4:16:06 PM

Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad VR1-1(1020mil,1480mil) on Multi-Layer And Track (929.448mil,1519.37mil)(1305.434mil,1519.37mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [7.874mil]
Waived by Matthew Matusek at 11/7/2019 4:16:16 PM

Silk To Solder Mask Clearance Constraint: (9.78mil < 10mil) Between Pad VR1-2(1118.426mil,1480mil) on Multi-Layer And Track (929.448mil,1519.37mil)(1305.434mil,1519.37mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.78mil]
Waived by Matthew Matusek at 11/7/2019 4:16:23 PM

Silk To Solder Mask Clearance Constraint: (9.78mil < 10mil) Between Pad VR1-3(1216.85mil,1480mil) on Multi-Layer And Track (929.448mil,1519.37mil)(1305.434mil,1519.37mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.78mil]
Waived by Matthew Matusek at 11/7/2019 4:16:28 PM

Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad VR2-1(240.001mil,1480mil) on Multi-Layer And Track (149.449mil,1519.37mil)(525.433mil,1519.37mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [7.874mil]
Waived by Matthew Matusek at 11/7/2019 4:16:38 PM

Silk To Solder Mask Clearance Constraint: (9.78mil < 10mil) Between Pad VR2-2(338.425mil,1480mil) on Multi-Layer And Track (149.449mil,1519.37mil)(525.433mil,1519.37mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.78mil]
Waived by Matthew Matusek at 11/7/2019 4:16:44 PM

Silk To Solder Mask Clearance Constraint: (9.78mil < 10mil) Between Pad VR2-3(436.851mil,1480mil) on Multi-Layer And Track (149.449mil,1519.37mil)(525.433mil,1519.37mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.78mil]
Waived by Matthew Matusek at 11/7/2019 4:16:49 PM

Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad VR3-1(1020mil,2280mil) on Multi-Layer And Track (929.448mil,2319.37mil)(1305.434mil,2319.37mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [7.874mil]
Waived by Matthew Matusek at 11/7/2019 4:16:58 PM

Silk To Solder Mask Clearance Constraint: (9.78mil < 10mil) Between Pad VR3-2(1118.426mil,2280mil) on Multi-Layer And Track (929.448mil,2319.37mil)(1305.434mil,2319.37mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.78mil]
Waived by Matthew Matusek at 11/7/2019 4:17:02 PM

Silk To Solder Mask Clearance Constraint: (9.78mil < 10mil) Between Pad VR3-3(1216.85mil,2280mil) on Multi-Layer And Track (929.448mil,2319.37mil)(1305.434mil,2319.37mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.78mil]
Waived by Matthew Matusek at 11/7/2019 4:17:06 PM

Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad VR4-1(600mil,3280mil) on Multi-Layer And Track (509.449mil,3319.37mil)(885.433mil,3319.37mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [7.874mil]
Waived by Matthew Matusek at 11/7/2019 4:17:20 PM

Silk To Solder Mask Clearance Constraint: (9.78mil < 10mil) Between Pad VR4-2(698.425mil,3280mil) on Multi-Layer And Track (509.449mil,3319.37mil)(885.433mil,3319.37mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.78mil]
Waived by Matthew Matusek at 11/7/2019 4:17:16 PM

Silk To Solder Mask Clearance Constraint: (9.78mil < 10mil) Between Pad VR4-3(796.85mil,3280mil) on Multi-Layer And Track (509.449mil,3319.37mil)(885.433mil,3319.37mil) on Top Overlay [Top Overlay] to [Top Solder] clearance [9.78mil]
Waived by Matthew Matusek at 11/7/2019 4:17:12 PM

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Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)

Height Constraint: DIP Component S1-DPDT Switch (200mil,2680mil) on Top Layer Actual Height = 1019.291mil
Waived by Matthew Matusek at 11/7/2019 4:03:40 PM

Height Constraint: Small Component S2-SPDT Switch (1700mil,2750mil) on Top Layer Actual Height = 1102.362mil
Waived by Matthew Matusek at 11/7/2019 4:03:47 PM

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