

# Lecture 18: Project Layout

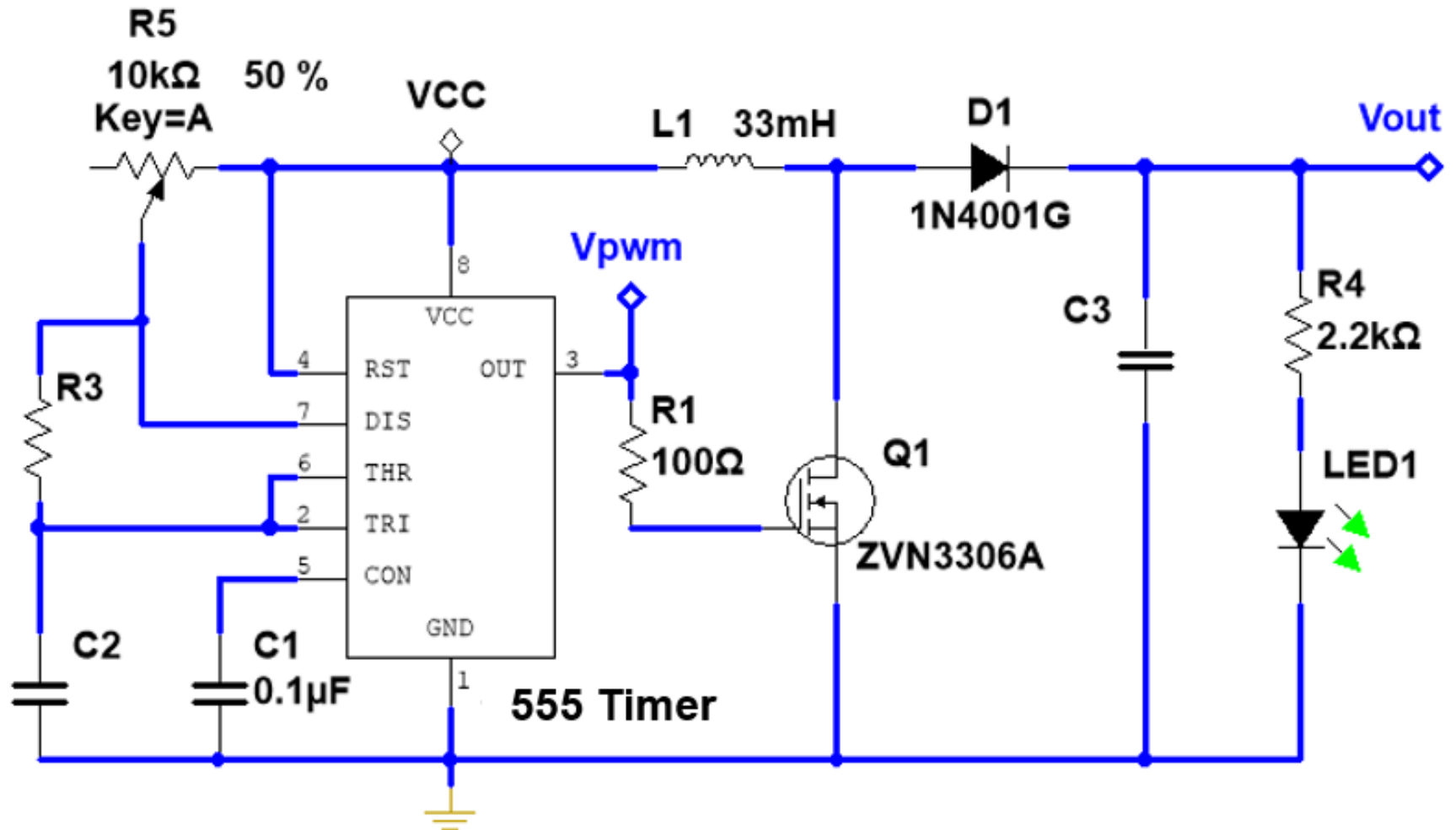
Instructor: Adam Barnes

Office: Thornton E206

Email: [ab6uy@virginia.edu](mailto:ab6uy@virginia.edu)

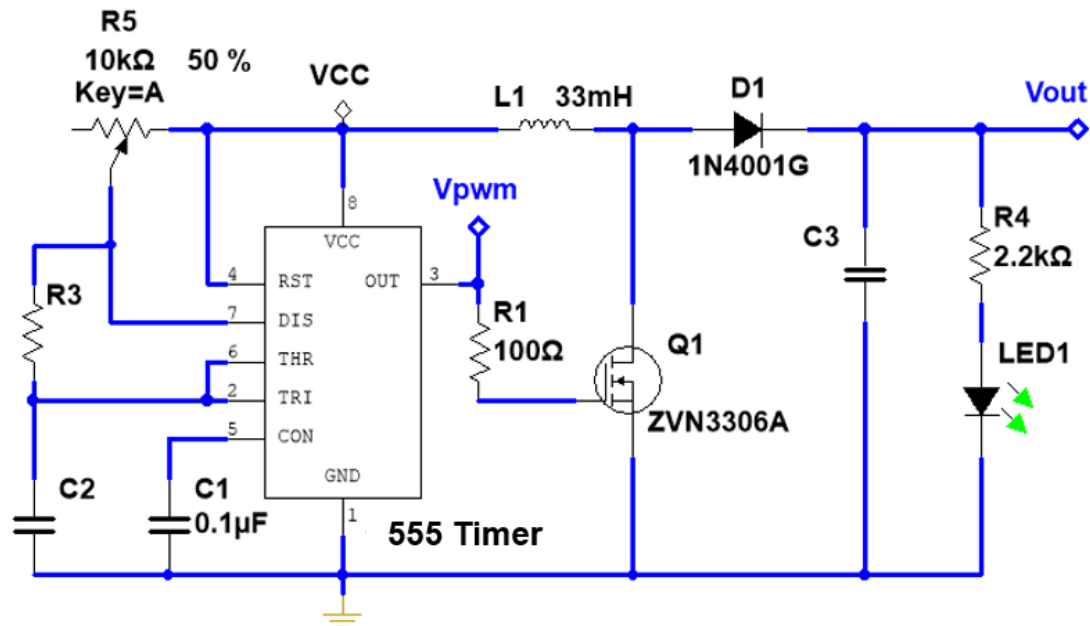
# Final Project Problem

- Design a boost converter to step 5V up to 13V



# Final Project Problem

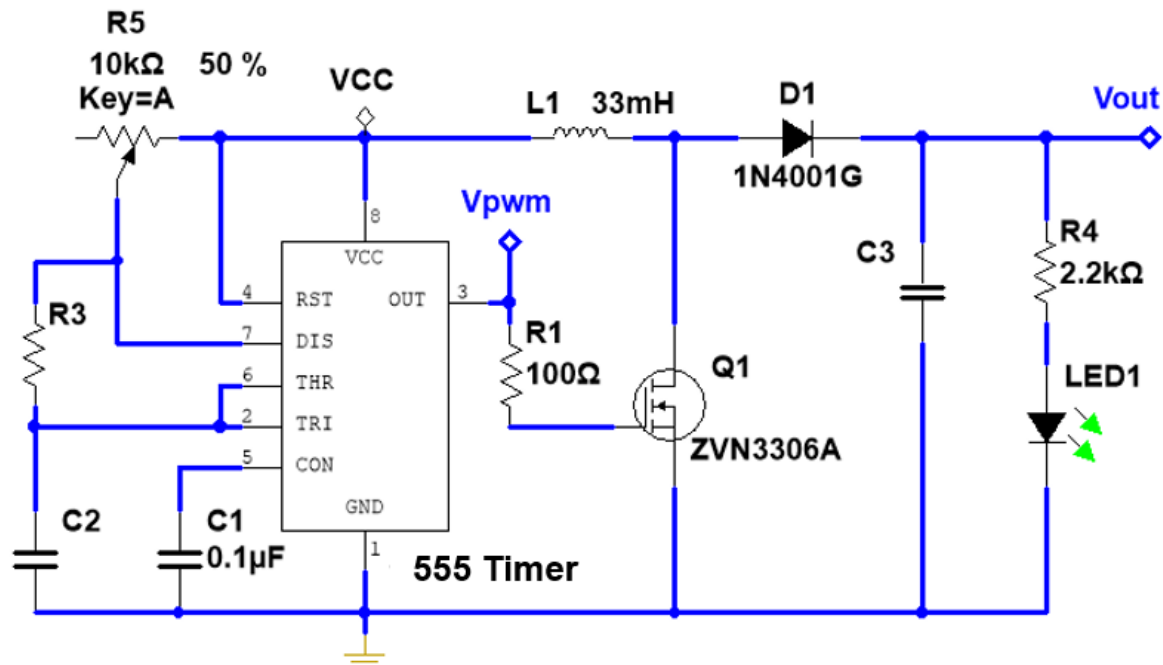
- The frequency of the PWM signal is adjustable with the  $10\text{k}\Omega$  potentiometer, but should have a duty cycle between 50% and 80%. For testing purposes we will set the frequency to 1kHz.
- The boost converter should be able to maintain at least 13V within 0.3% across a load consisting of an LED in series with a  $2.2\text{k}\Omega$  resistor.



# Breaking the problem down

- Find the value of R3 based on the duty cycle between 50% and 80%

$$D = \frac{T_{on}}{T_{total}} = \frac{R_A + R_B}{R_A + 2R_B}$$



# Breaking the problem down

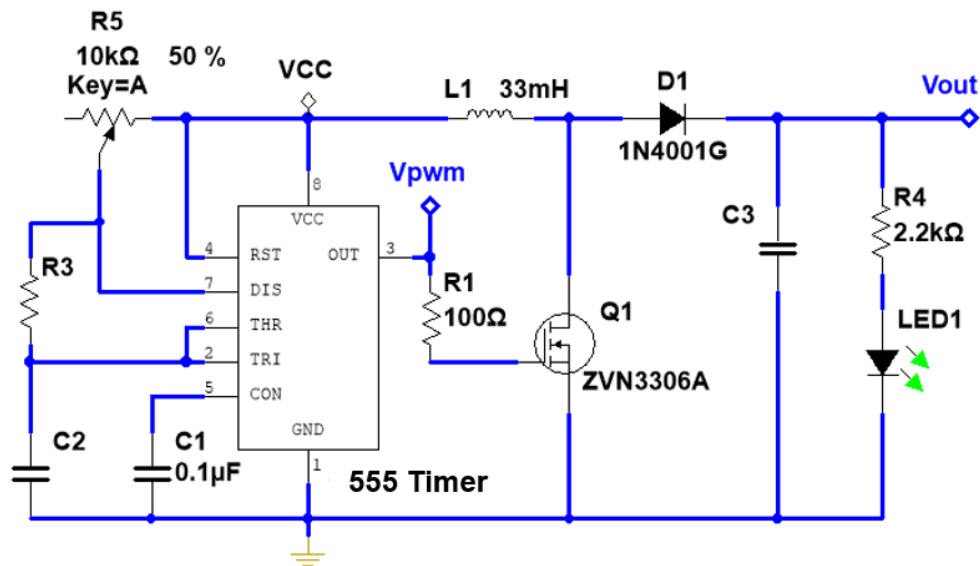
- Once we have R3, we can use the frequency specification to set C2

$$T_{on} = 0.693(R_A + R_B)C$$

$$T_{off} = 0.693R_B C$$

$$T_{total} = T_{on} + T_{off} = 0.693(R_A + 2R_B)C \quad f = \frac{1}{T_{total}}$$

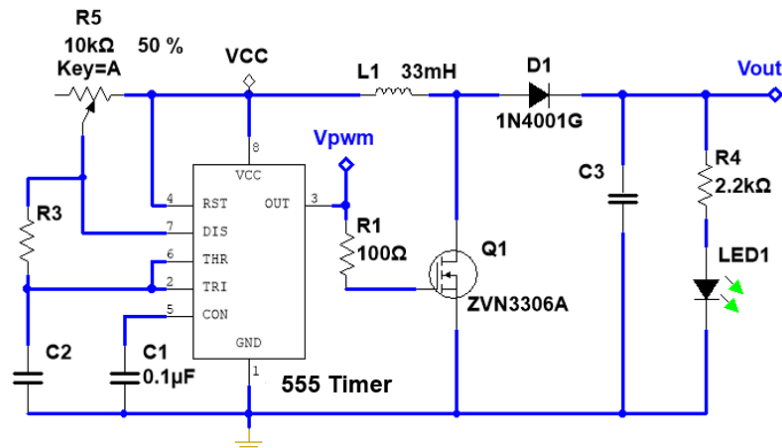
We have a range of 0 to 10kΩ for the pot; we need to pick a capacitor value in our kit that will give us a 1ms period with  $0 < R_A < 10\text{k}\Omega$



# Breaking the problem down

- To find C3 we need to calculate the power absorbed by the load and make sure C3 is large enough to maintain 13V when it has to supply the current to the load.
- How much energy does the resistor absorb?
- How much energy does the LED absorb?
- How much charge does the capacitor lose during the off cycle?

This is very similar to the problem in HW2e



# Breaking the problem down

- To find the energy in the inductor, we need to know the current when the switch is open.
- We can use KVL to find an equation for that:

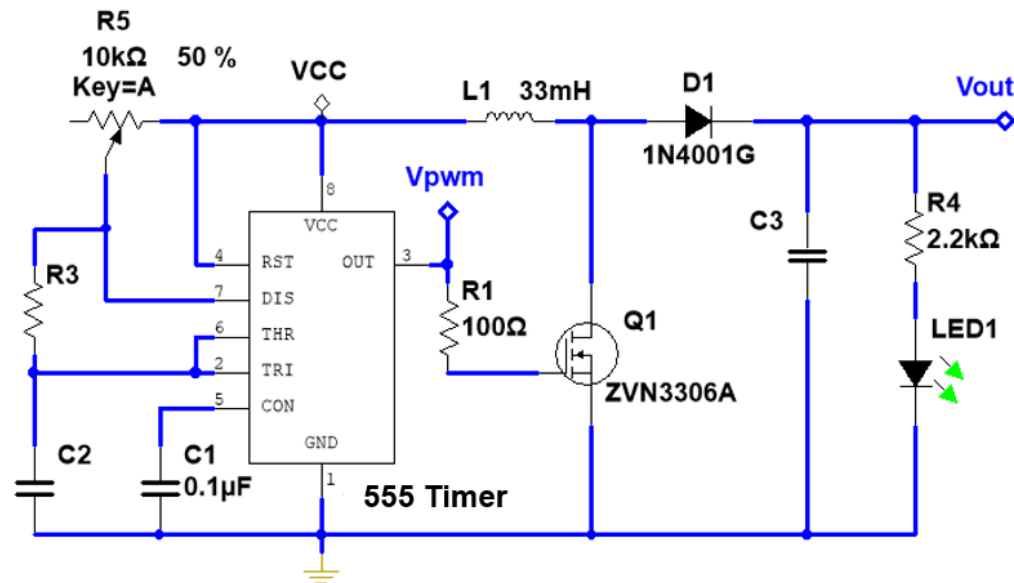
$$-V_{CC} + v_L + iR_L + v_{DS} = 0$$

$V_{CC}$  = supply voltage

$v_L$  = inductor voltage

$iR_L$  = voltage across  
inductor resistance

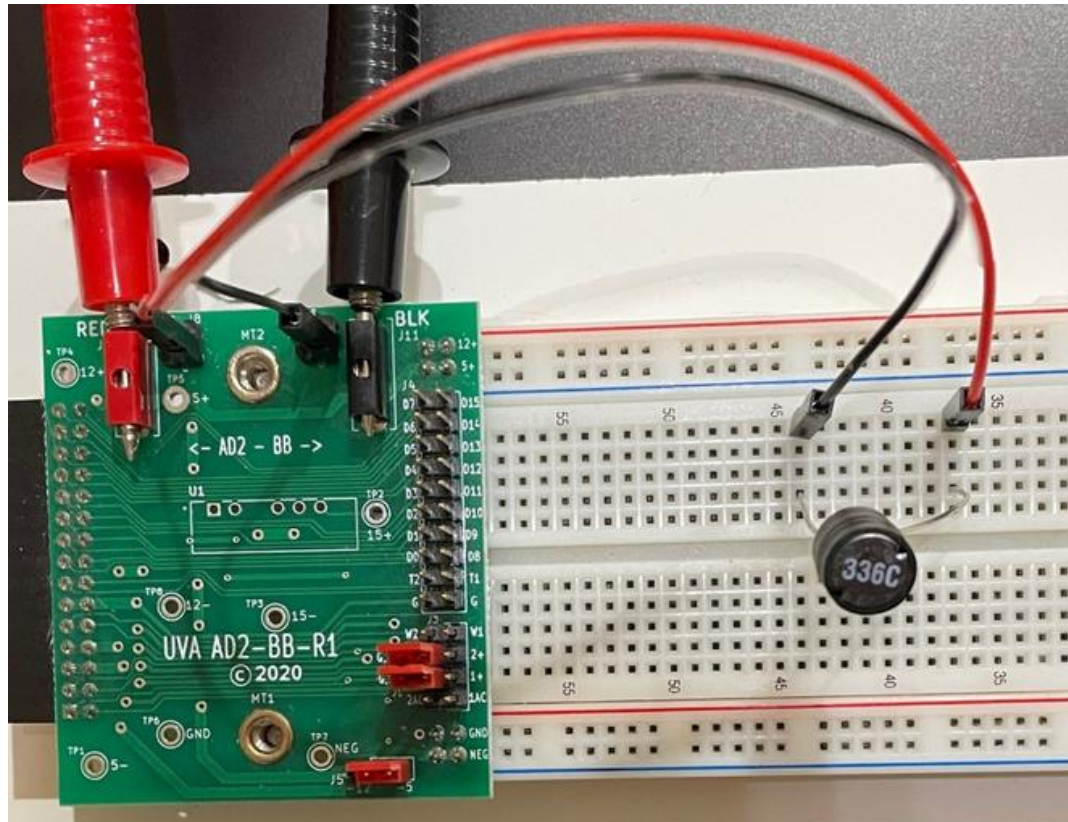
$v_{DS}$  = drain-source voltage  
across transistor



You will need to measure the resistance of your inductor with your multimeter

# Measuring the inductor

- Measure your inductor properly! Do not just hold the multimeter probes against the inductor leads!
- Your final calculations will be sensitive to this value.





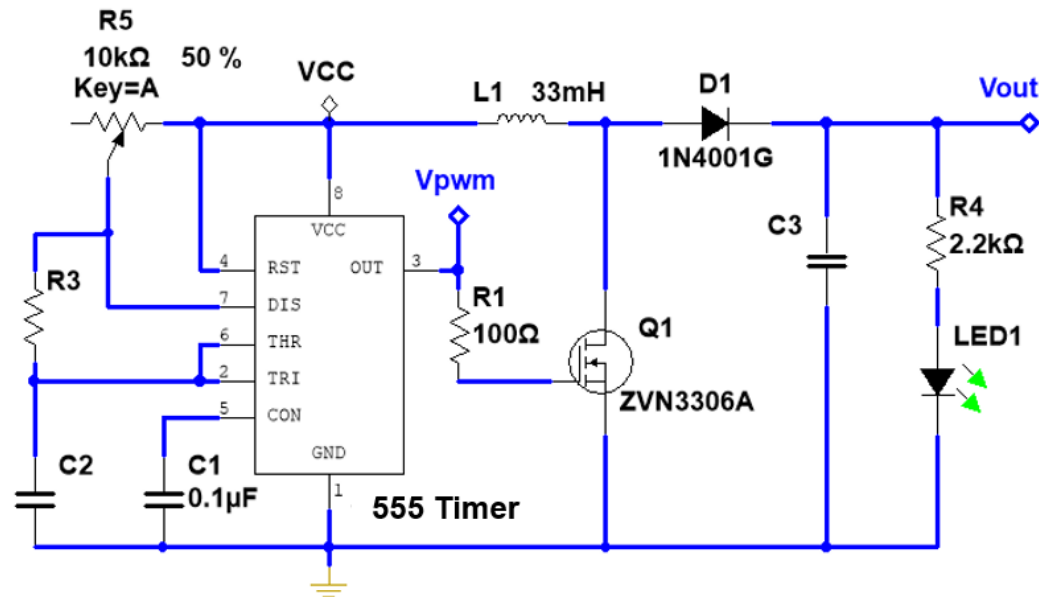
# Breaking the problem down

- Now put in terms of the current to create a differential equation which we can solve to find  $i(t)$

$$-V_{CC} + v_L + iR_L + v_{DS} = 0$$

$$v_L = L \frac{di}{dt}$$

$$\frac{L}{R_L} \frac{di}{dt} + i(t) = \frac{V_{CC} - v_{DS}}{R_L}$$



# Breaking the problem down

- We also need to determine a value for  $v_{DS}$  so we have values for all our variables. Since we are in the triode region, we can use the equation:

$$v_{DS} = (v_{GS} - V_t) + \frac{1}{R_D K_n} \pm \sqrt{\left[ (v_{GS} - V_t) + \frac{1}{R_D K_n} \right]^2 - \frac{2V_{DD}}{R_D K_n}}$$

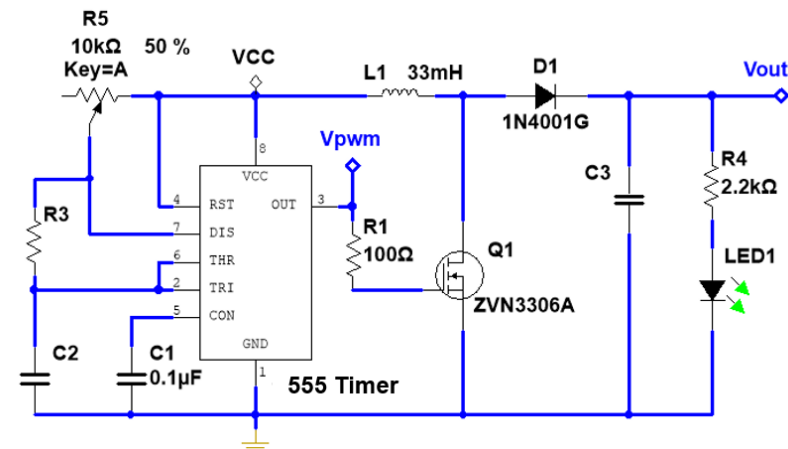
In this case, we have

$$R_D = R_L$$

$$V_{DD} = V_{CC} = 5V$$

$$V_t = 1.824V \quad \text{Threshold voltage}$$

$$K_n = 0.1233 \frac{A}{V^2} \quad \text{MOSFET transconductance parameter}$$



# Breaking down the problem

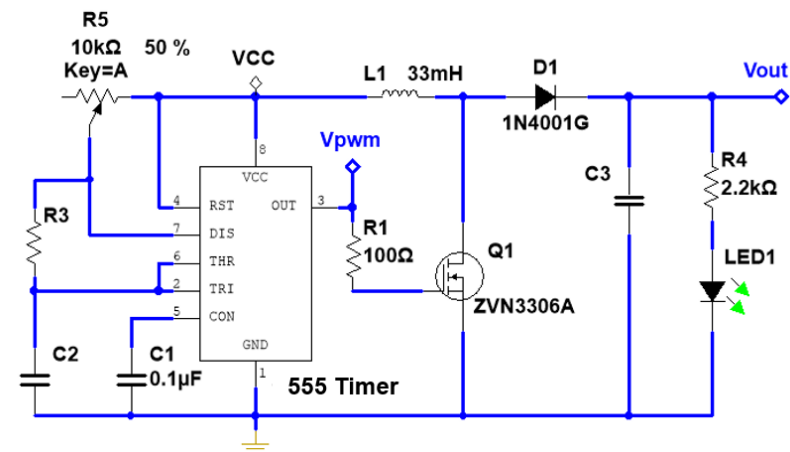
- Once we have an equation for the current, we can determine the energy the inductor stores during each 'on' cycle and compare it to the amount of energy the load uses each full cycle.

$$p(t) = v_L(t)i(t) = L \frac{di(t)}{dt} i(t)$$

$$v_L(t) = L \frac{di(t)}{dt}$$

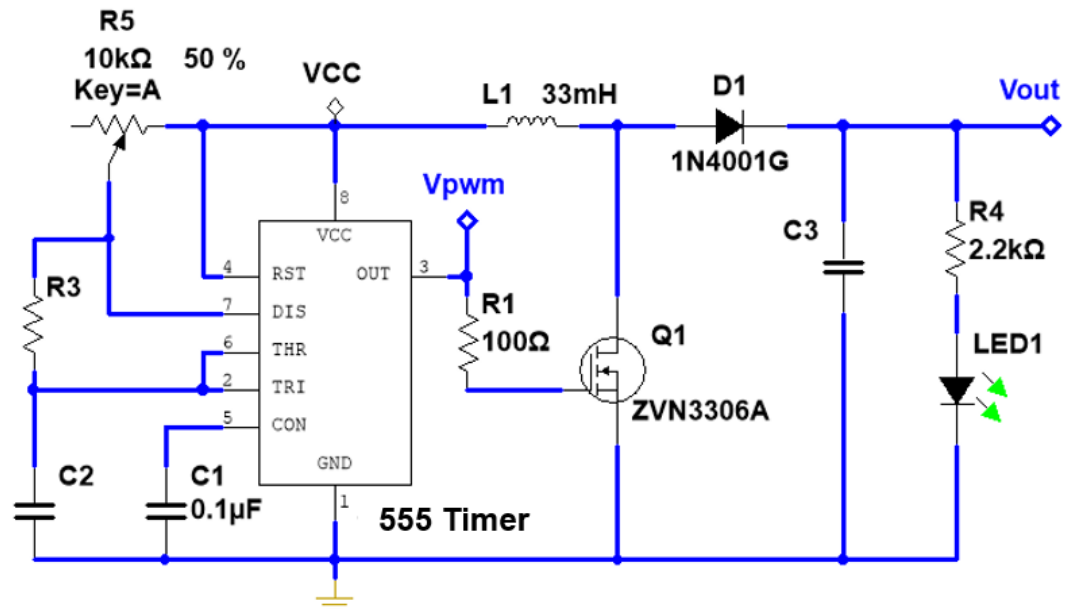
$$w(t) = \int_0^{T_{on}} p(t) dt = \int_0^{T_{on}} L \frac{di(t)}{dt} i(t) dt$$

$$w(t) = L \int_0^{T_{on}} i(t) di$$



# Project Milestone 1 Submission

- Calculate values for R3, C2, and C3 and submit to Gradescope
  - Show calculations and final values
  - This should be typed up so that it is easy to read and so you can just cut and paste it into your final report
- You should complete these calculations before laying out your printed circuit board



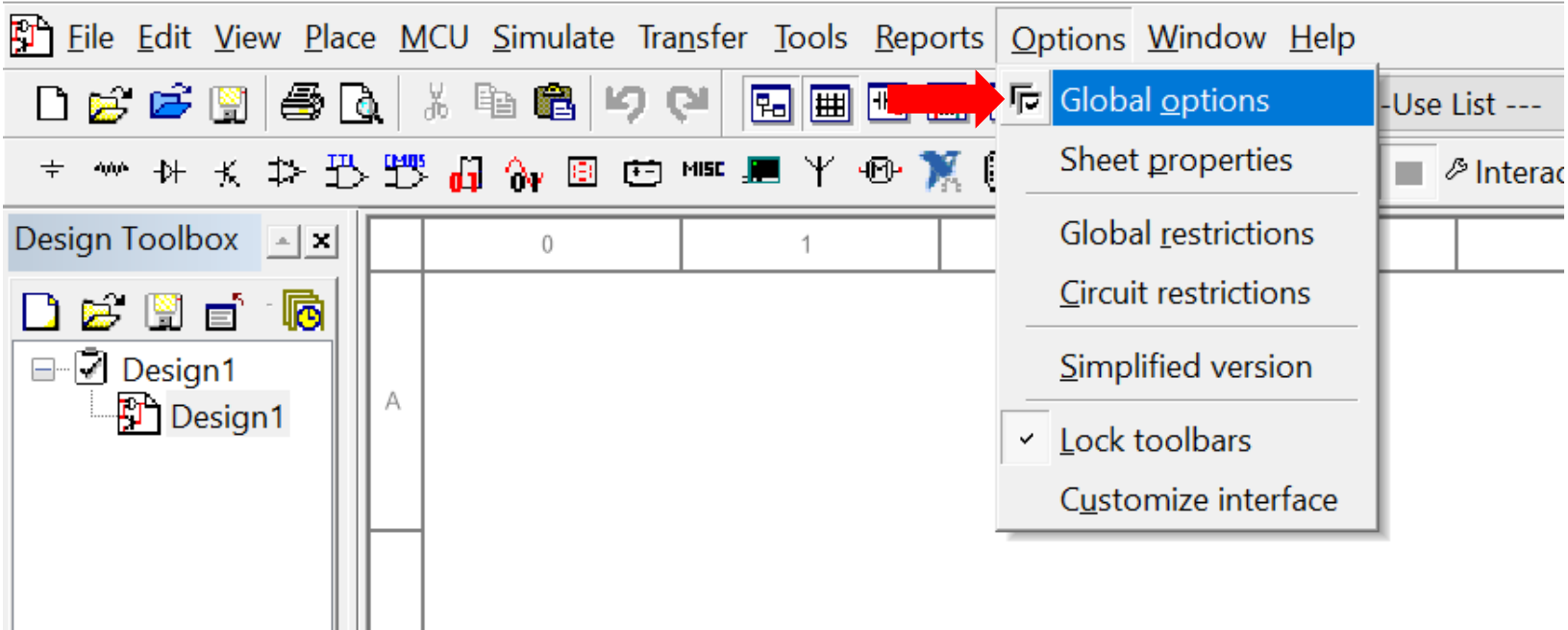
# Multisim & Ultiboard

**If you want to make your life hard when setting up the project PCB, skip this lecture**

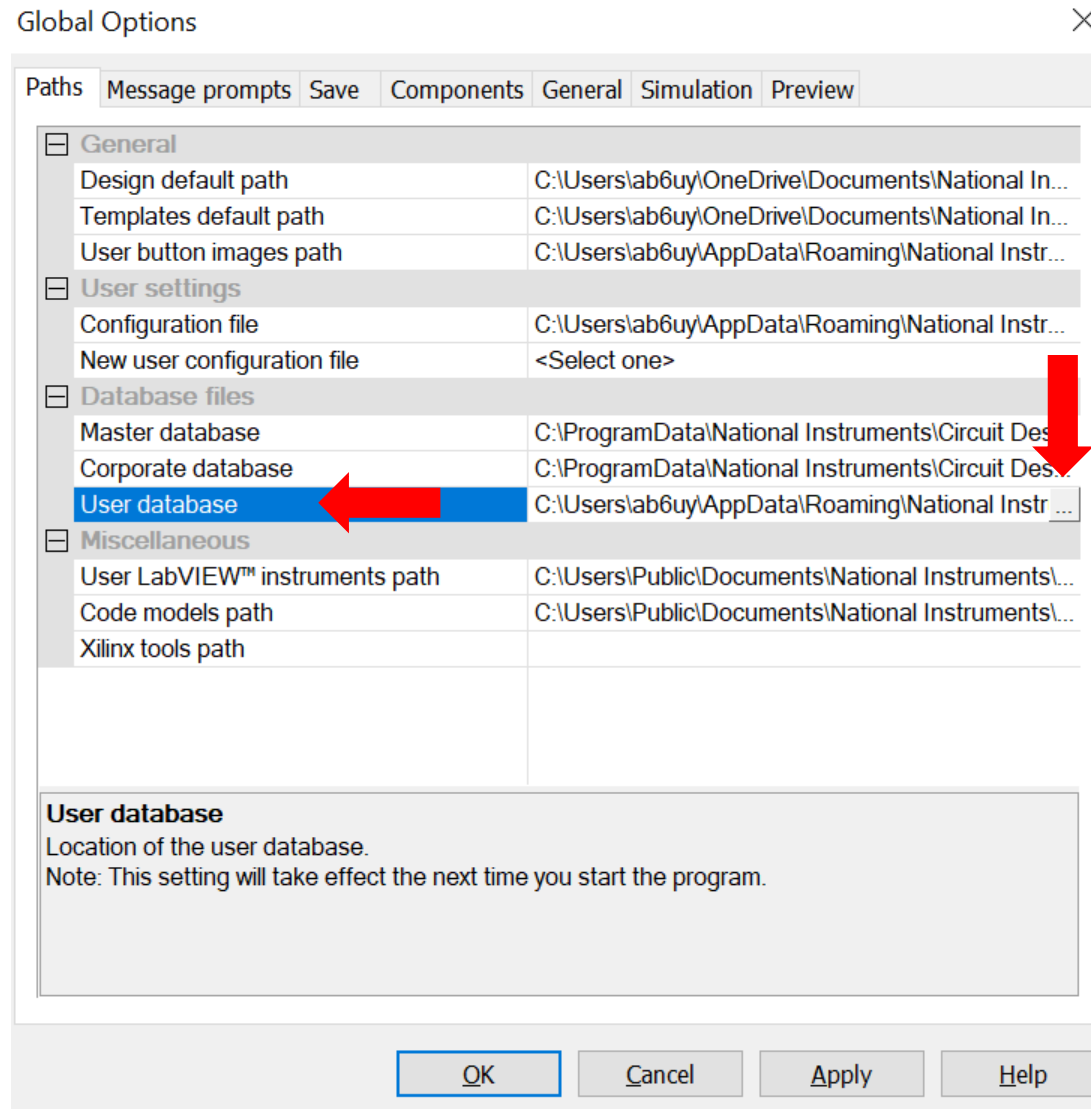
# Defining User Library in Multisim

- Download Library files from Collab and save them in a folder where you will be able to locate them.
- Then open Multisim and select Options>Global Options

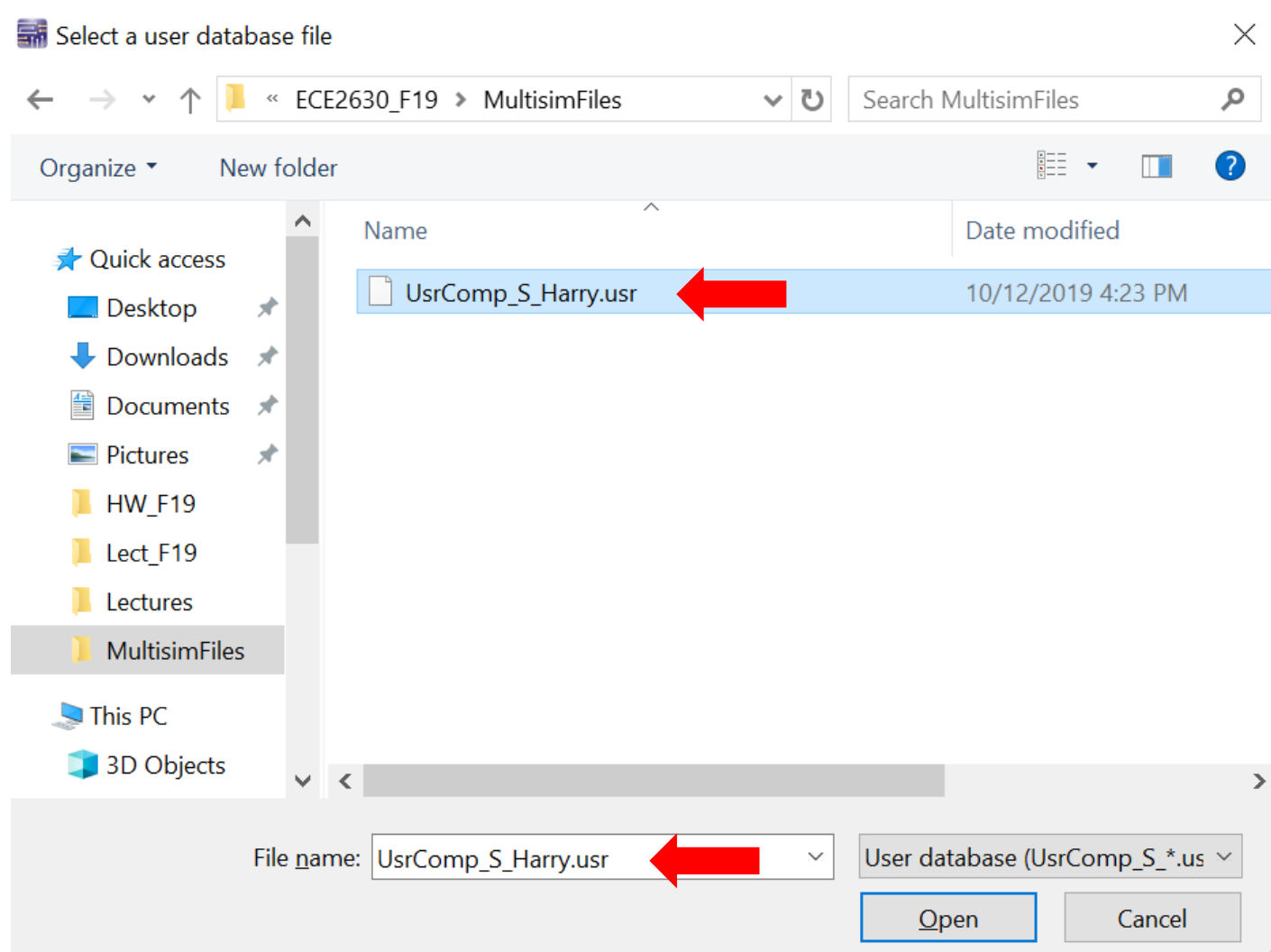
Design1 - Multisim - [Design1]



# Defining User Library in Multisim



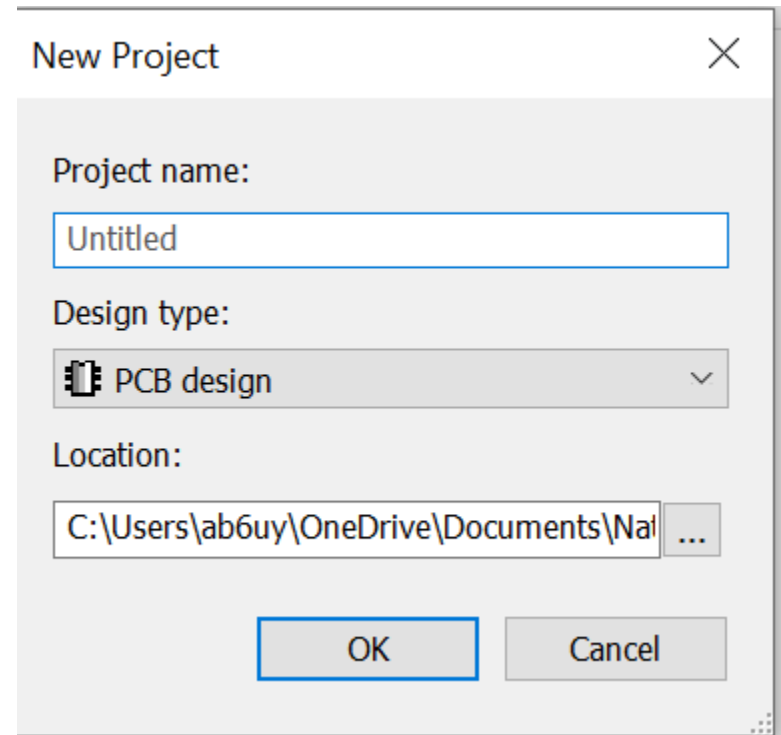
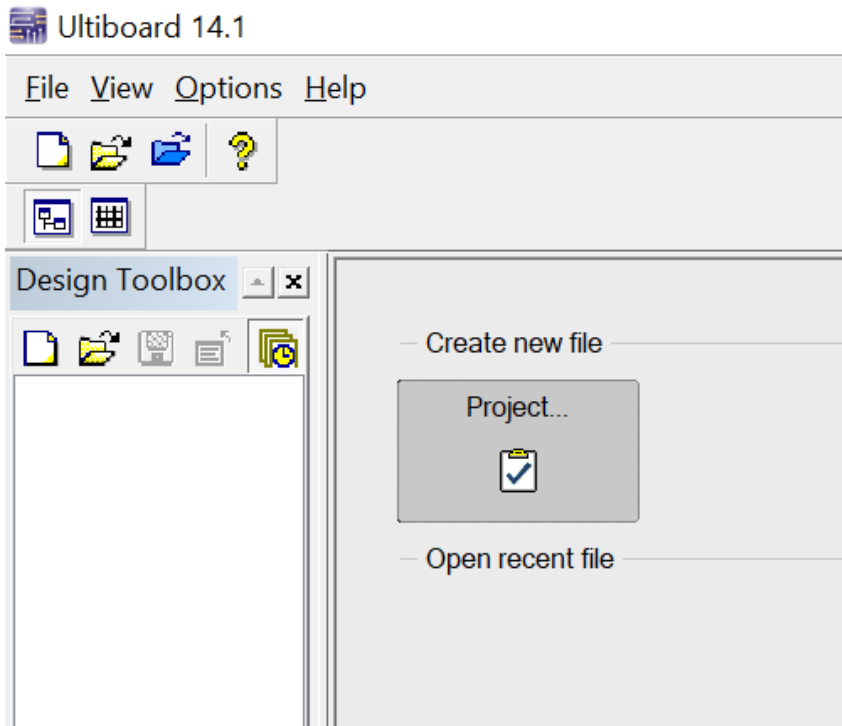
# Defining User Library in Multisim





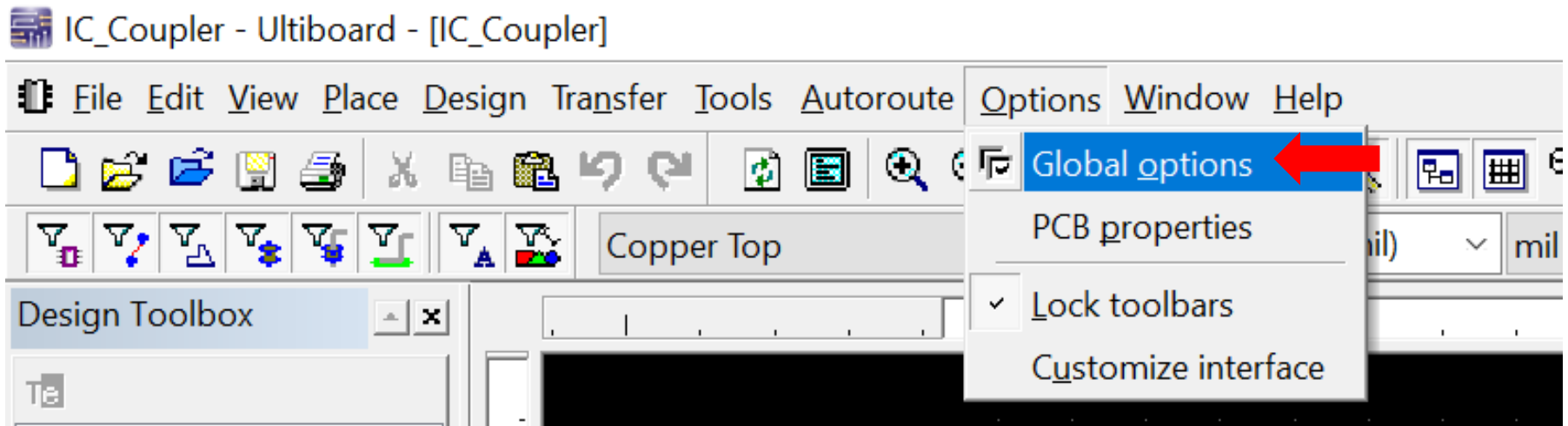
# Defining User Library in Ultiboard

- Next, open Ultiboard and create a New Project

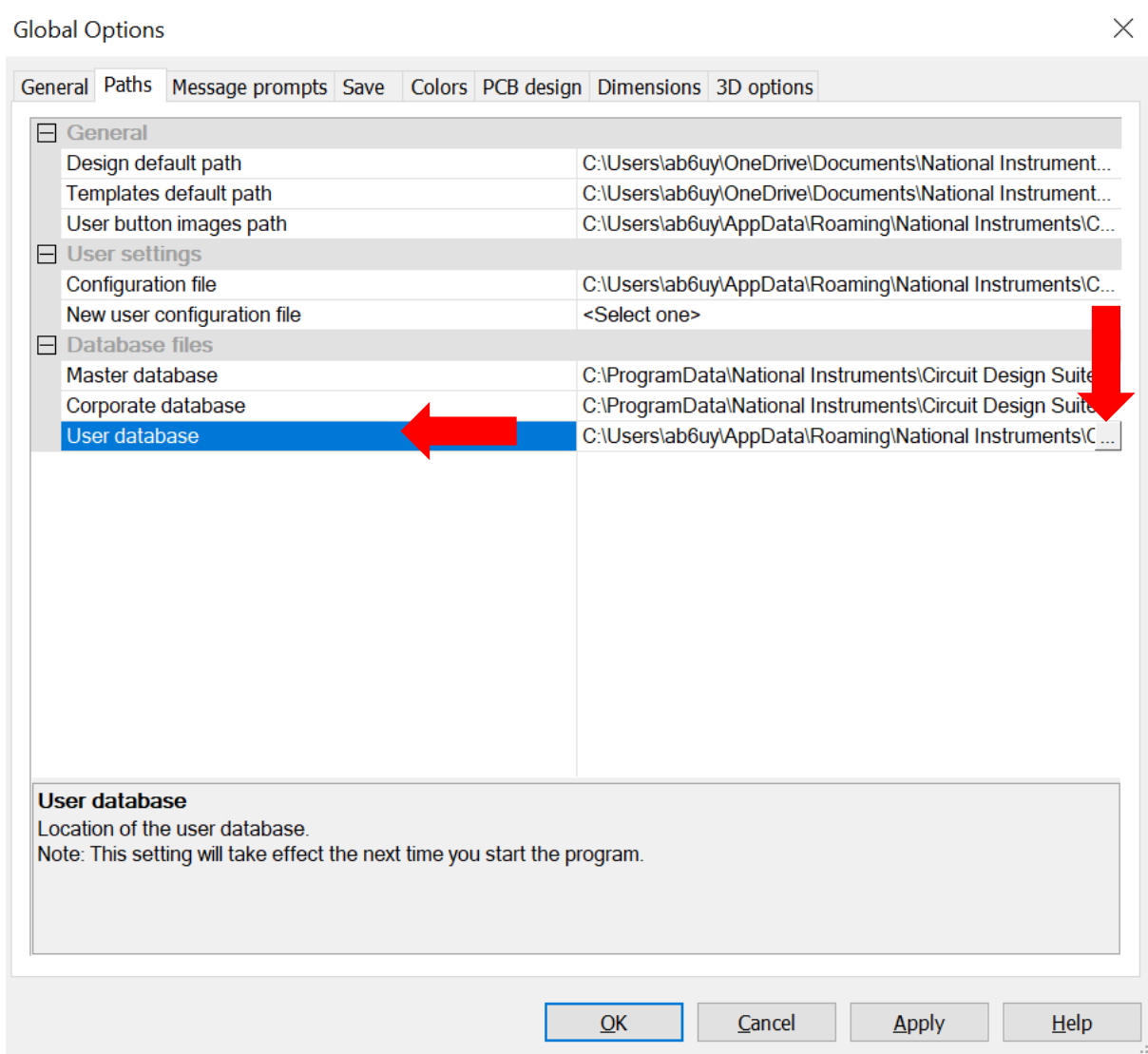


# Defining User Library in Ultiboard

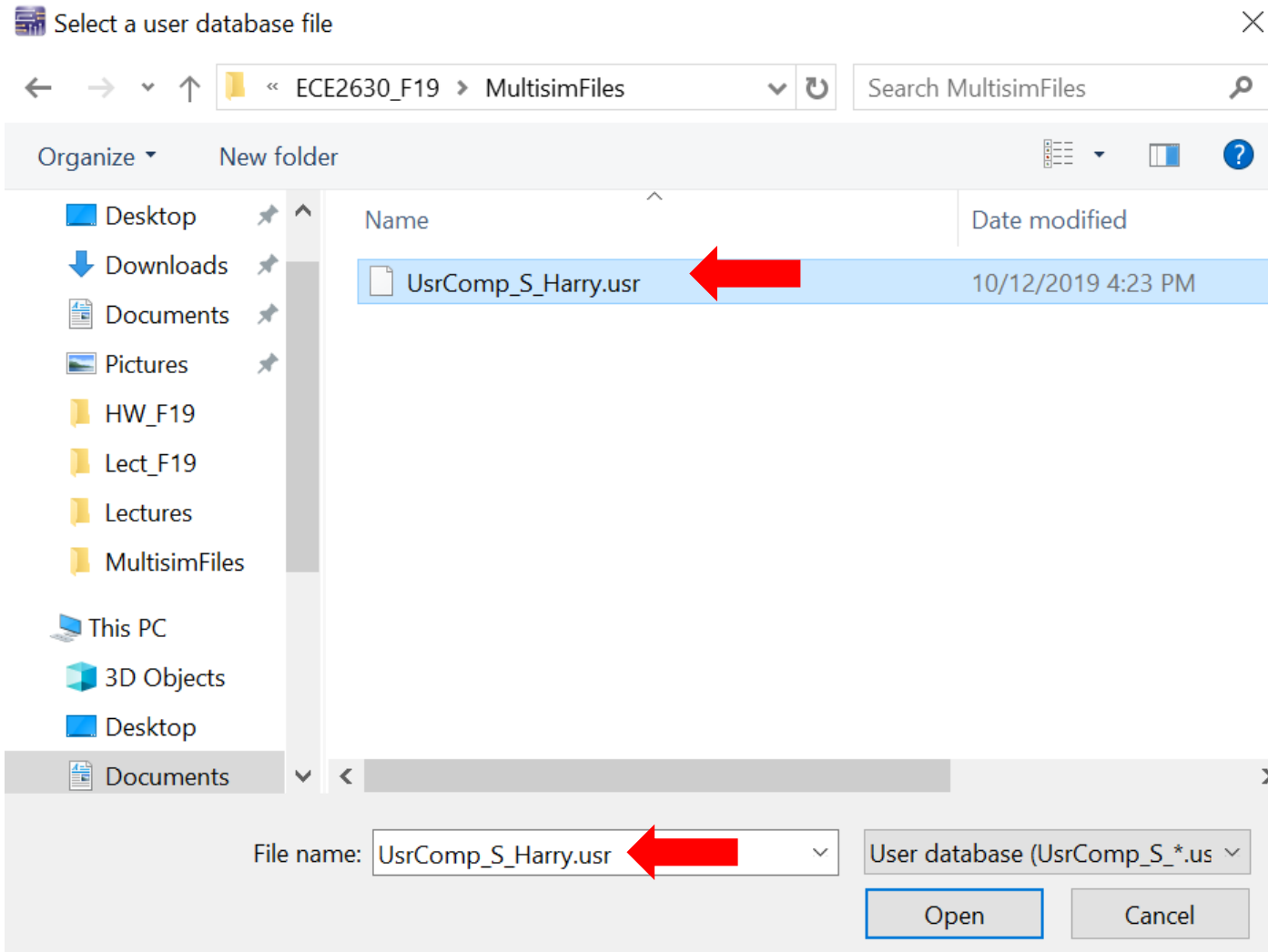
- Select Options>Global Options



# Defining User Library in Ultiboard

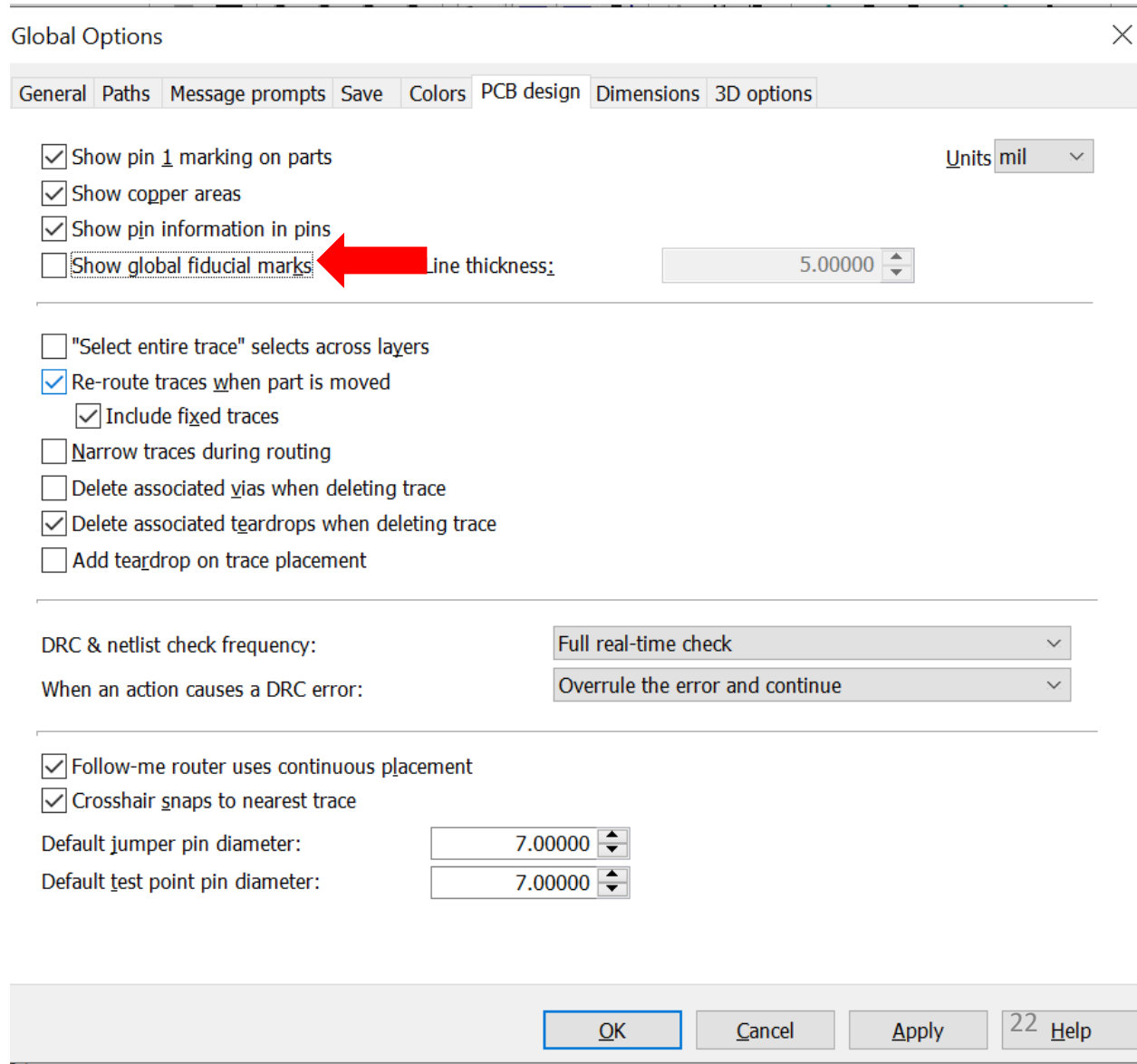


# Defining User Library in Ultiboard



# One More Setting to change...

- Under the Options menu, select Global Options
- Deselect Show global fiducial marks



The screenshot shows the 'Global Options' dialog box with the 'PCB design' tab selected. A red arrow points to the 'Show global fiducial marks' checkbox, which is currently unchecked. Other settings visible include 'Show pin 1 marking on parts' (checked), 'Show copper areas' (checked), 'Show pin information in pins' (checked), 'Line thickness' (5.00000), 'Re-route traces when part is moved' (checked), 'Include fixed traces' (checked), 'Narrow traces during routing' (unchecked), 'Delete associated vias when deleting trace' (unchecked), 'Delete associated teardrops when deleting trace' (checked), 'Add teardrop on trace placement' (unchecked), 'DRC & netlist check frequency' (Full real-time check), 'When an action causes a DRC error' (Overrule the error and continue), 'Follow-me router uses continuous placement' (checked), 'Crosshair snaps to nearest trace' (checked), 'Default jumper pin diameter' (7.00000), and 'Default test point pin diameter' (7.00000). The 'Units' are set to 'mil'.

Global Options

General Paths Message prompts Save Colors PCB design Dimensions 3D options

☒ Show pin 1 marking on parts Units: mil

☒ Show copper areas

☒ Show pin information in pins

☐ Show global fiducial marks Line thickness: 5.00000

☐ "Select entire trace" selects across layers

☒ Re-route traces when part is moved

☒ Include fixed traces

☐ Narrow traces during routing

☐ Delete associated vias when deleting trace

☒ Delete associated teardrops when deleting trace

☐ Add teardrop on trace placement

DRC & netlist check frequency: Full real-time check

When an action causes a DRC error: Overrule the error and continue

☒ Follow-me router uses continuous placement

☒ Crosshair snaps to nearest trace

Default jumper pin diameter: 7.00000

Default test point pin diameter: 7.00000

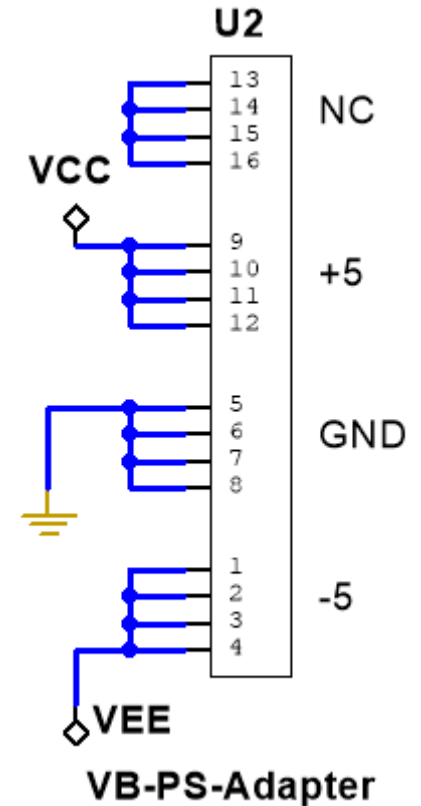
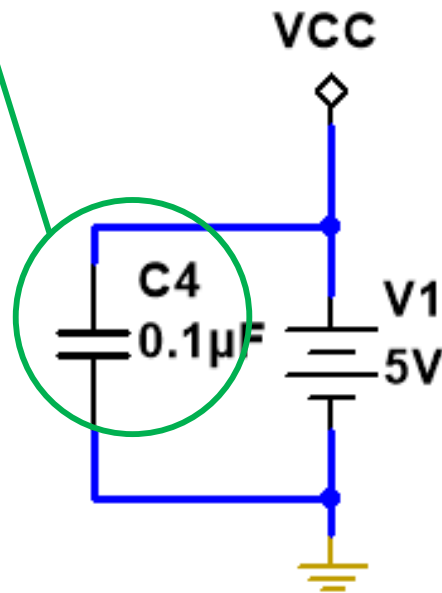
OK Cancel Apply Help

# Template File

- Close both Multisim & Ultiboard
- Download the template file (BoostConverterTemplate.mst14) to a folder where you will be able to find it.
- Double-click on the template file to open it.
- Both the schematic (in Multisim) and the board layout (in Ultiboard) should open. Eventually.

# Circuit Schematic Fixed Parts

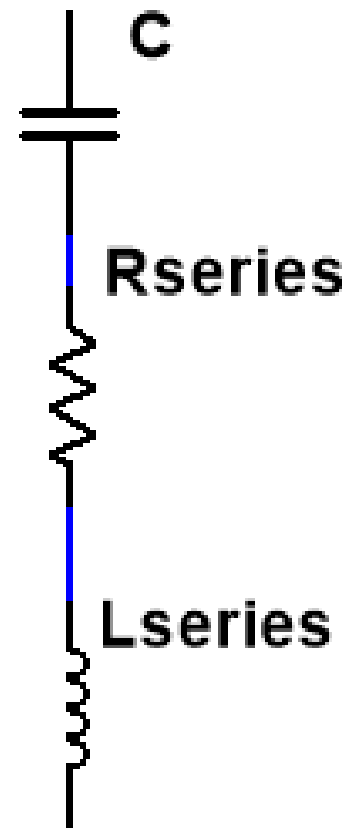
This bypass capacitor protects the circuit from transients in the power supply



This 'part' is just a place holder for header pins that will connect the PCB to the breadboard

# Bypass Capacitor Basics

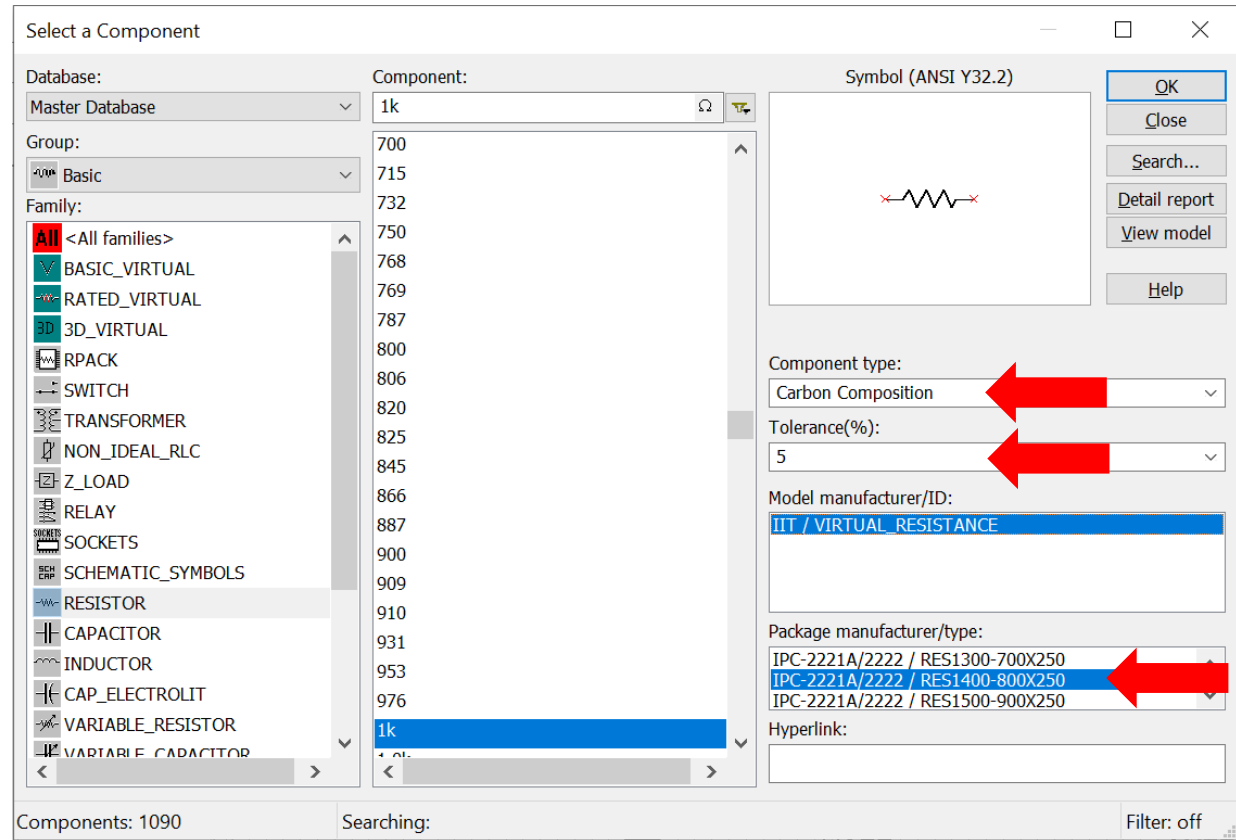
- Real capacitors have small inductance and resistances associated with them. These non-ideal values impact the impedance of the cap.
- Ceramic caps are typically used for bypass caps because they have low inductance and resistance compared with other types. Also they are cheap.
- The value of the bypass cap has to be large enough so it can store the charge generated by a transient – that is the high frequency voltage spikes caused by digital switching. Typically  $0.1\mu\text{F}$  is plenty big for this. Having a larger cap just lowers the base impedance which is nice by not necessarily critical.





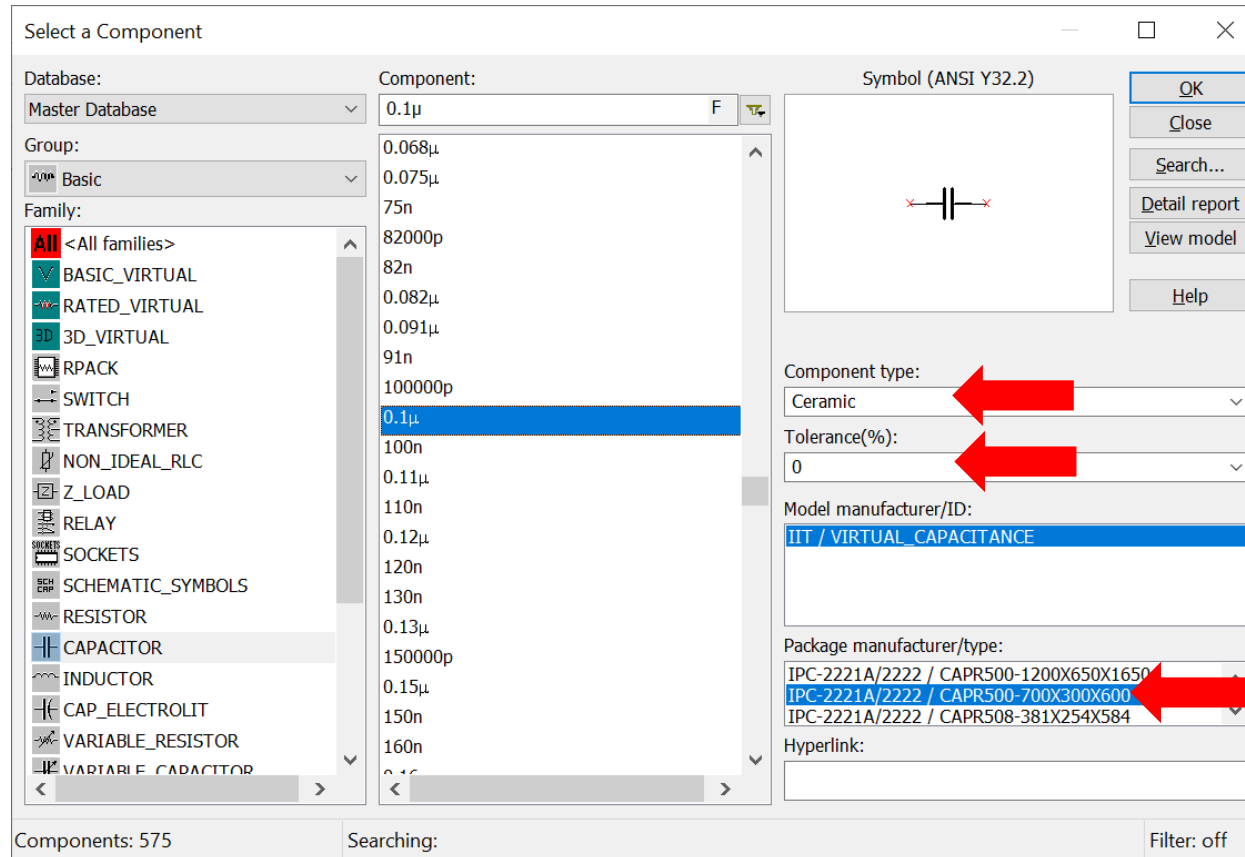
# Component Info

- Resistors
- 5% tolerance – Carbon composition
- Footprint  
Manufacturer/Type:  
IPC-2221A/2222  
RES1400-800X250

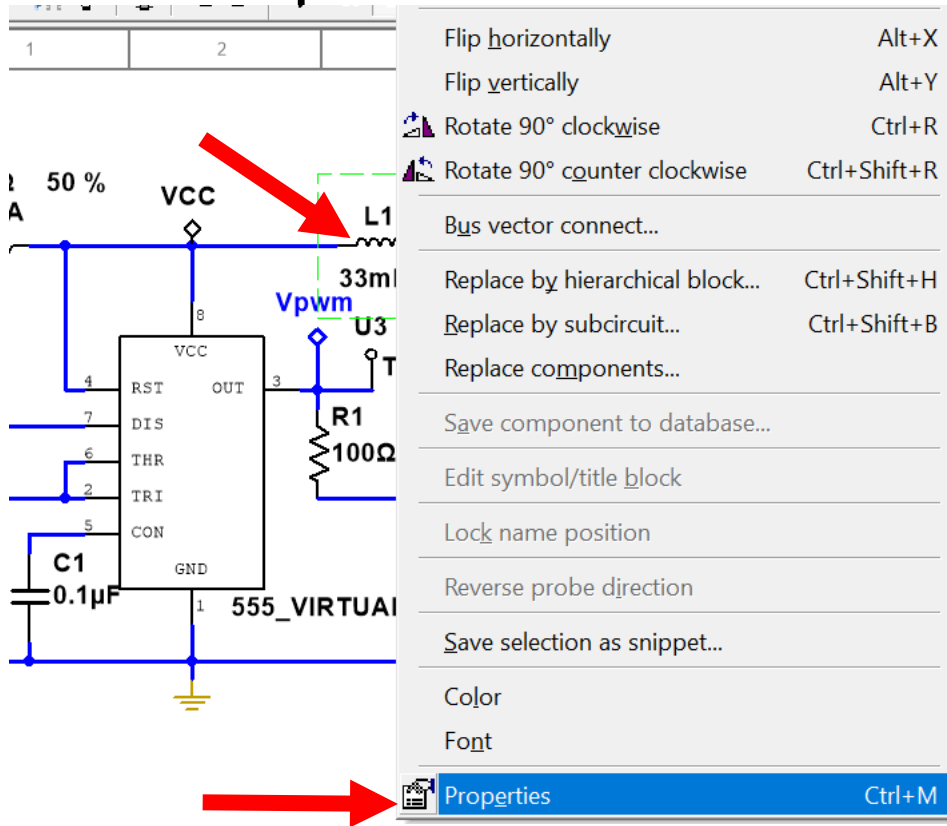


# Component Info

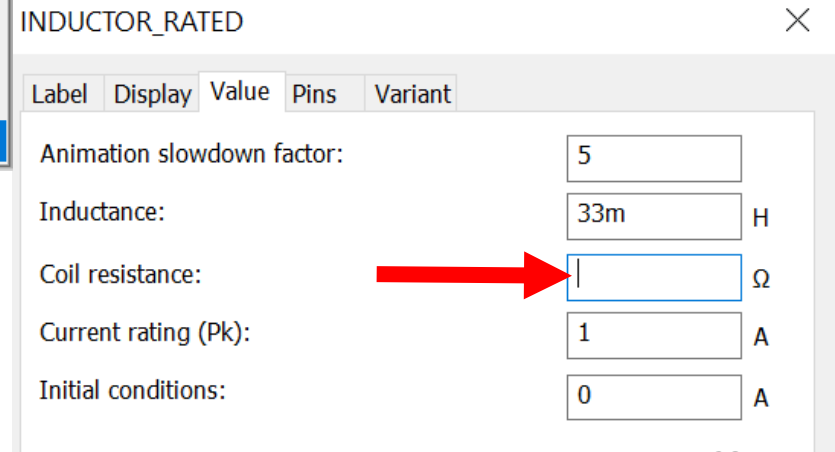
- Capacitors
- Tolerance: Unknown, so leave at 0%
- Ceramic
- Footprint  
Manufacturer/Type:  
IPC-2221A/2222  
CAPR500-  
700X300X600



# Component Info

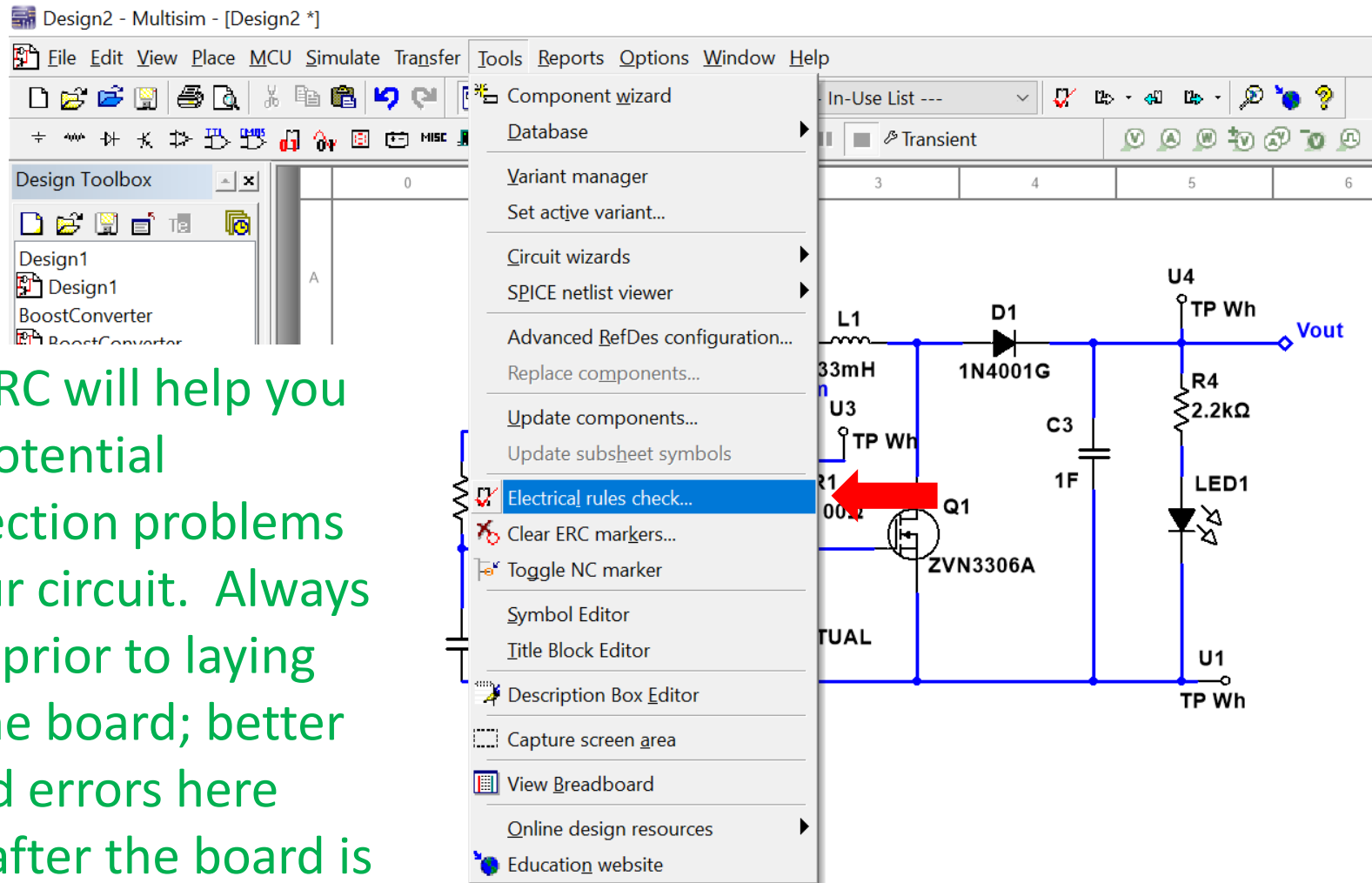


- Right click on the inductor
- Select Properties
- Set Coil Resistance to the value you measure with your Multimeter



# Run the Electrical Rules Check

The ERC will help you flag potential connection problems in your circuit. Always run it prior to laying out the board; better to find errors here than after the board is manufactured.



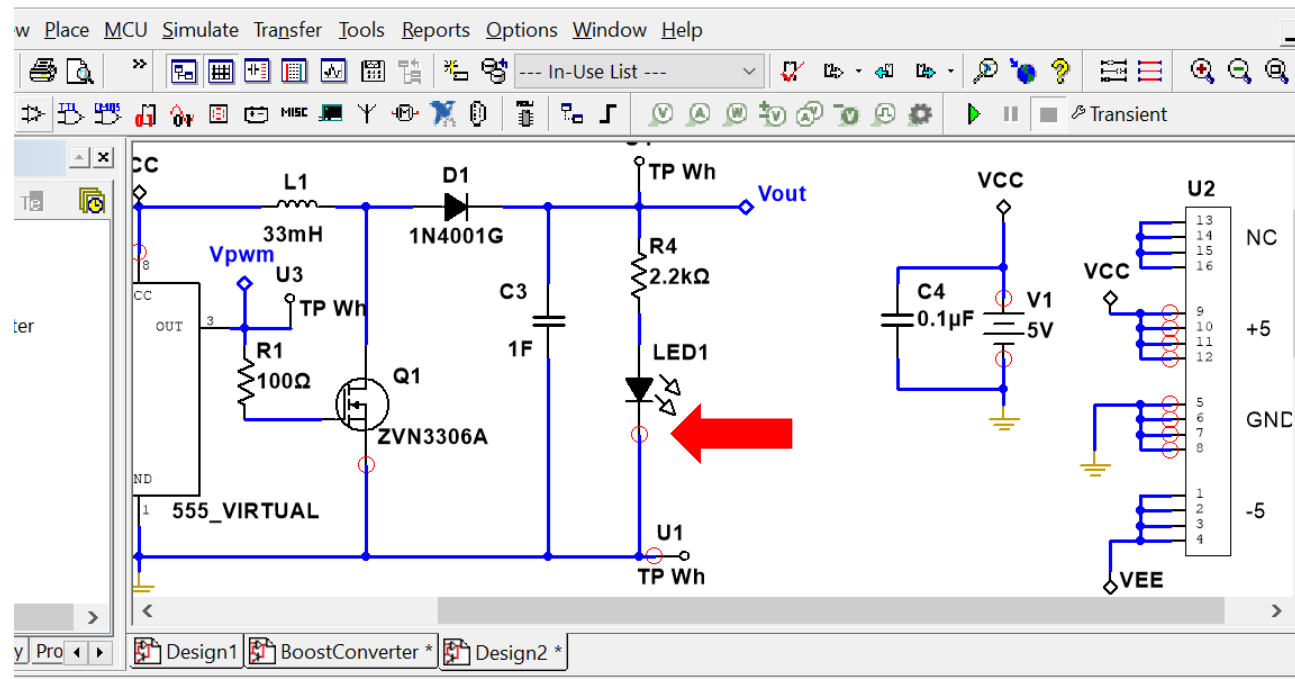
# Run the Electrical Rules Check

Oh \$#!+, errors!

Now what?

Each error shows up in a little red circle on the schematic.

A brief description of the error shows in the Results window.



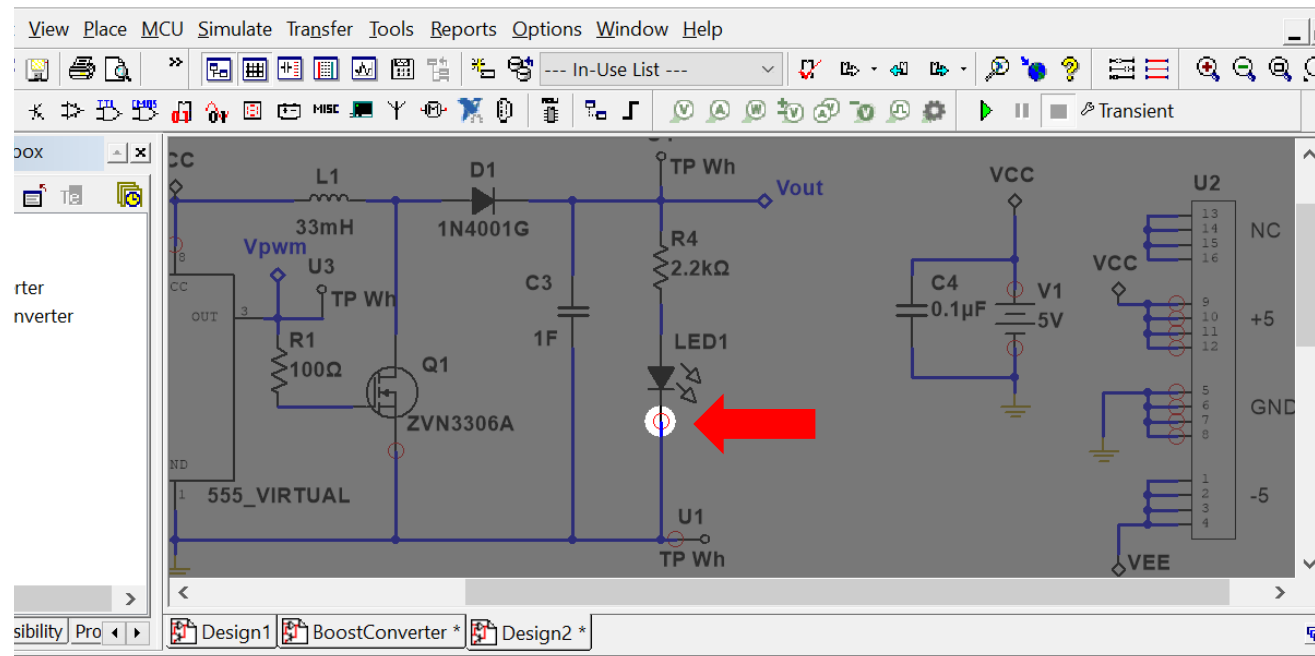
Connecting Power to Bidirectional: [A1 pin 8, Design2] to [U2 pin 11, Design2]  
Connecting Power to Bidirectional: [A1 pin 8, Design2] to [U2 pin 12, Design2]  
Connecting Power to Bidirectional: [V1 pin 1, Design2] to [U2 pin 9, Design2]  
Error: Connecting Power to Bidirectional: [V1 pin 1, Design2] to [U2 pin 10, Design2]  
Error: Connecting Power to Bidirectional: [V1 pin 1, Design2] to [U2 pin 11, Design2]  
Error: Connecting Power to Bidirectional: [V1 pin 1, Design2] to [U2 pin 12, Design2]

Completed; 15 error(s), 0 warning(s); Time: 0:00.14

# Run the Electrical Rules Check

You can double click on the error in the Results window to highlight its location in the circuit.

In this case all of our errors are mismatched pin types. Typically this prevent you from accidentally doing something like connecting the output pin directly to the power supply.



Error: Connecting Bidirectional to Power: [Q1 pin S, Design2] to [V1 pin 2, Design2]

Error: Connecting Bidirectional to Power: [LED1 pin K, Design2] to [V1 pin 2, Design2]

Error: Connecting Bidirectional to Power: [U1 pin 1, Design2] to [V1 pin 2, Design2]

Error: Connecting Bidirectional to Power: [U2 pin 5, Design2] to [V1 pin 2, Design2]

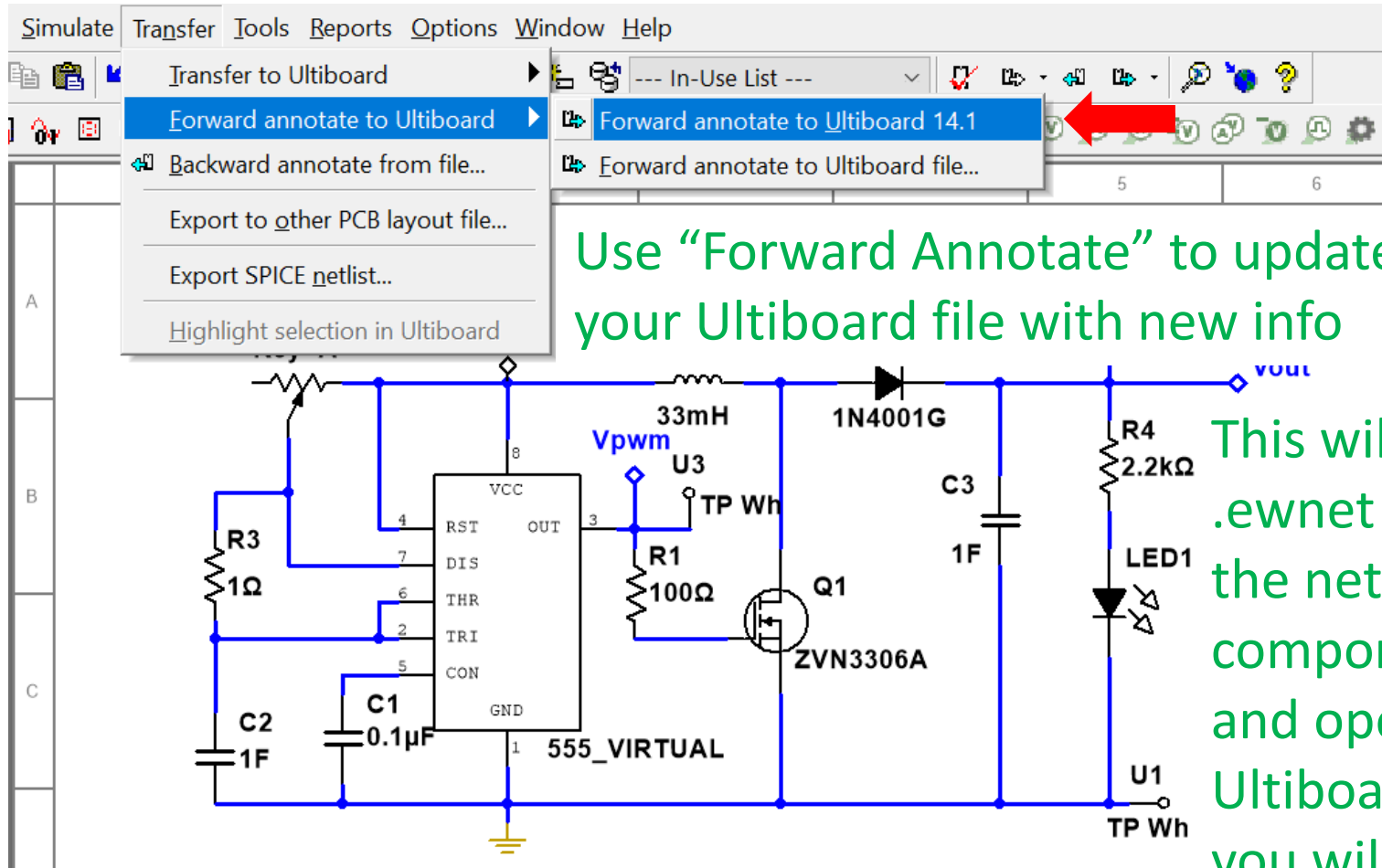
Error: Connecting Bidirectional to Power: [U2 pin 6, Design2] to [V1 pin 2, Design2]

Error: Connecting Bidirectional to Power: [U2 pin 8, Design2] to [V1 pin 2, Design2]

Error: Connecting Bidirectional to Power: [U2 pin 7, Design2] to [V1 pin 2, Design2]

Error: Connecting Power to Bidirectional: [A1 pin 8, Design2] to [U2 pin 9, Design2]

# Moving Multisim Data to Ultiboard



Use “Forward Annotate” to update your Ultiboard file with new info

This will create a .ewnet file that has the netlist and component info and open up Ultiboard where you will be prompted for your project file.

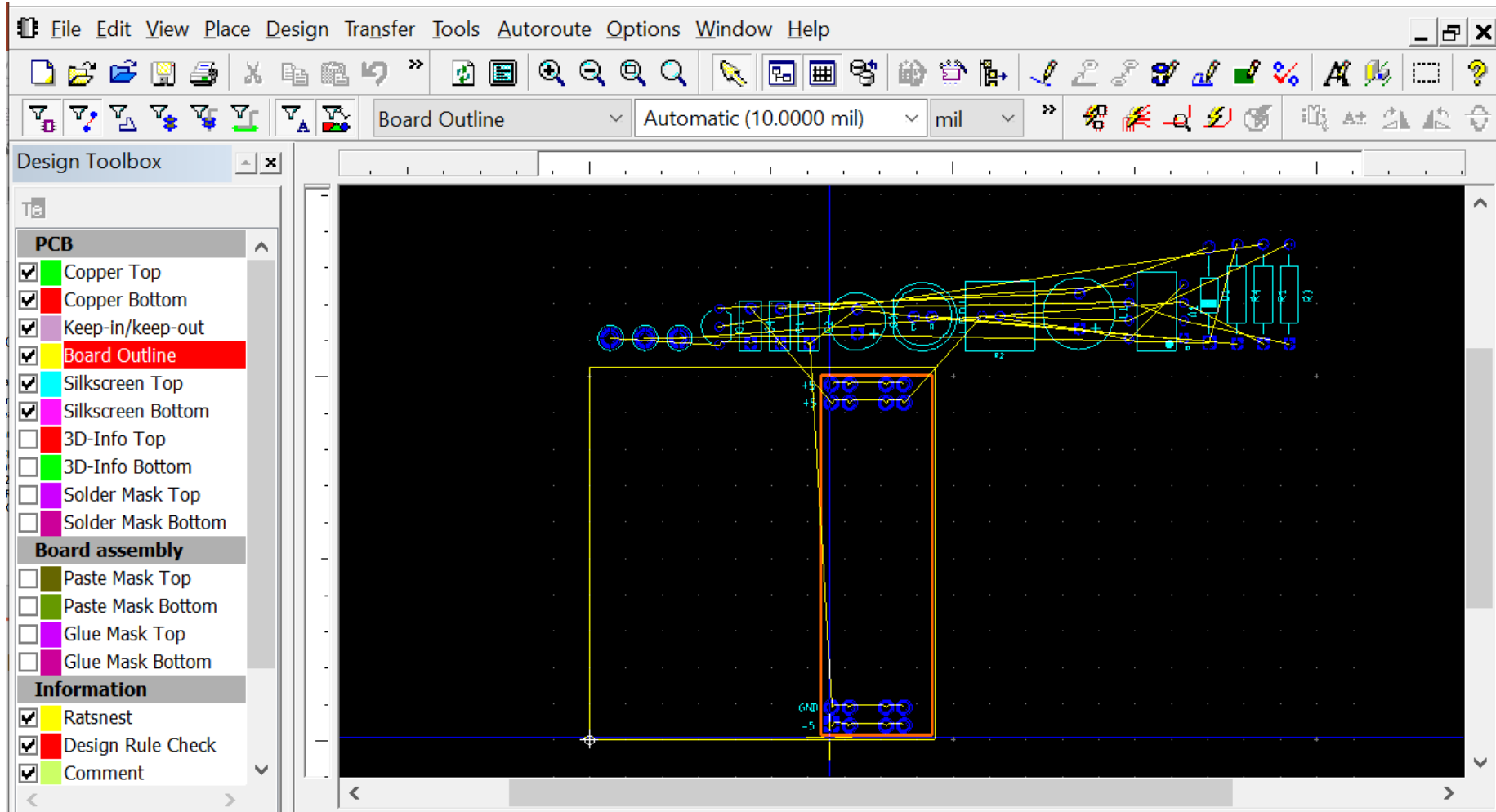
Do NOT use the “Transfer to Ultiboard” – that will reset everything in your Ultiboard file

# Ultiboard

**How to lay out a PCB**

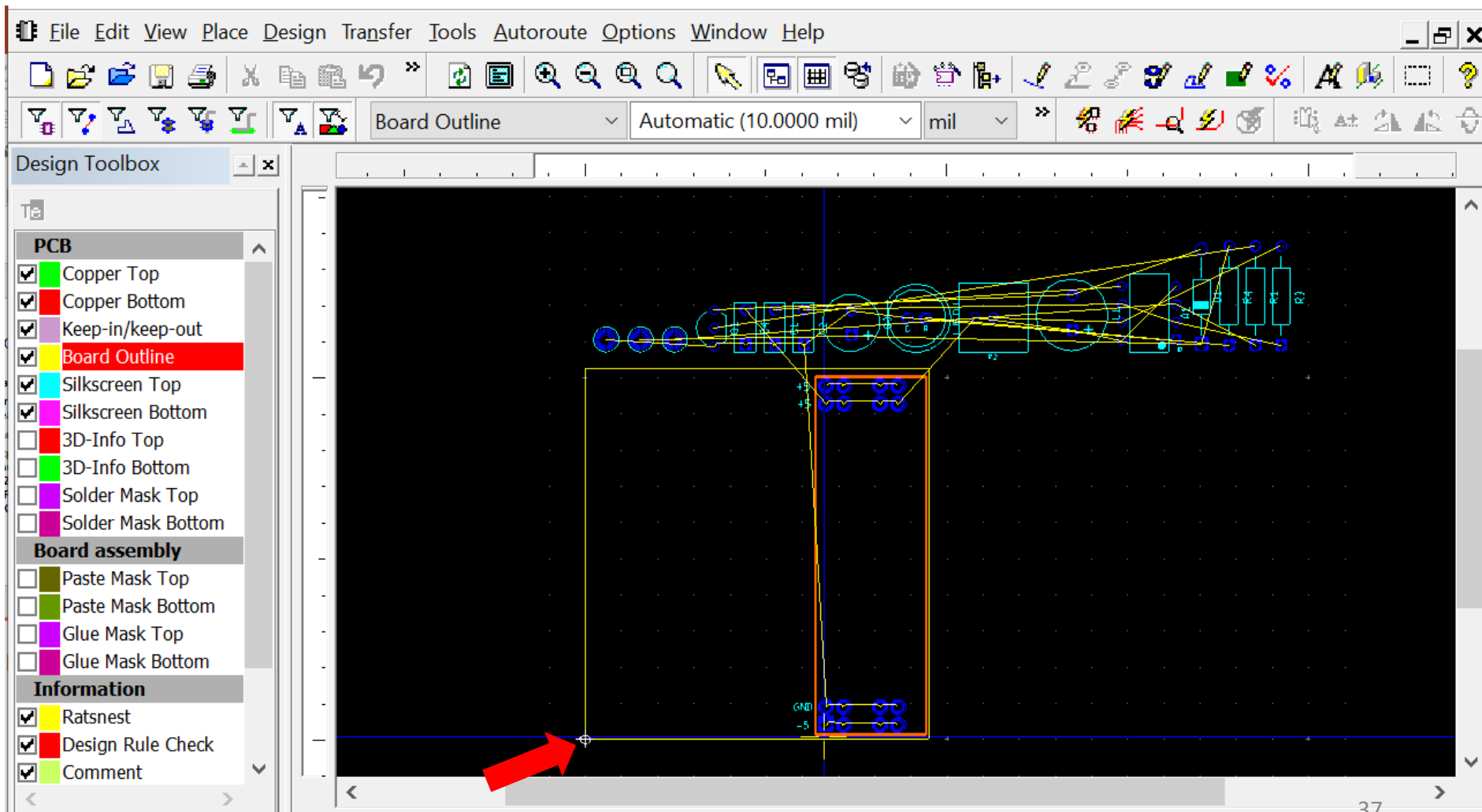


# Ultiboard



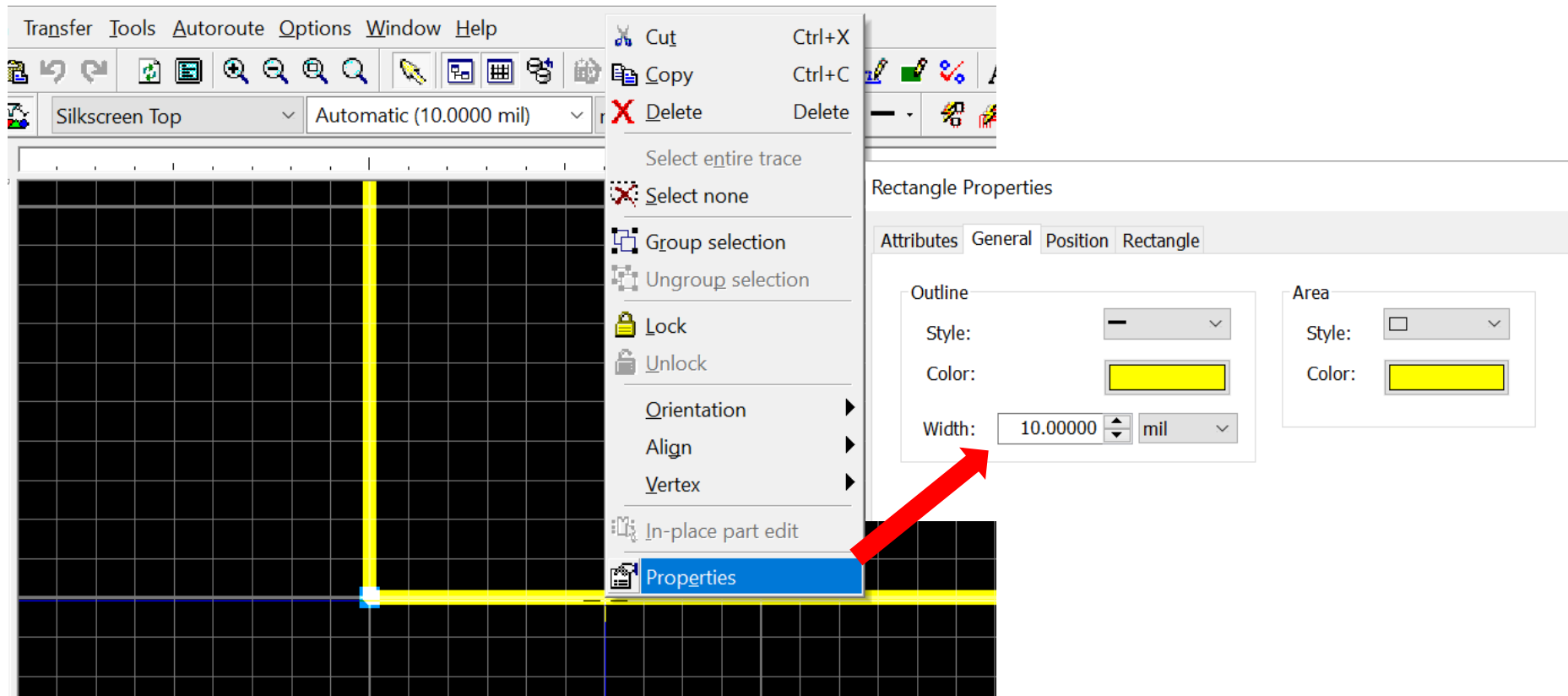
# Before you get started with the layout

- Check to make sure your lower left corner is at the origin



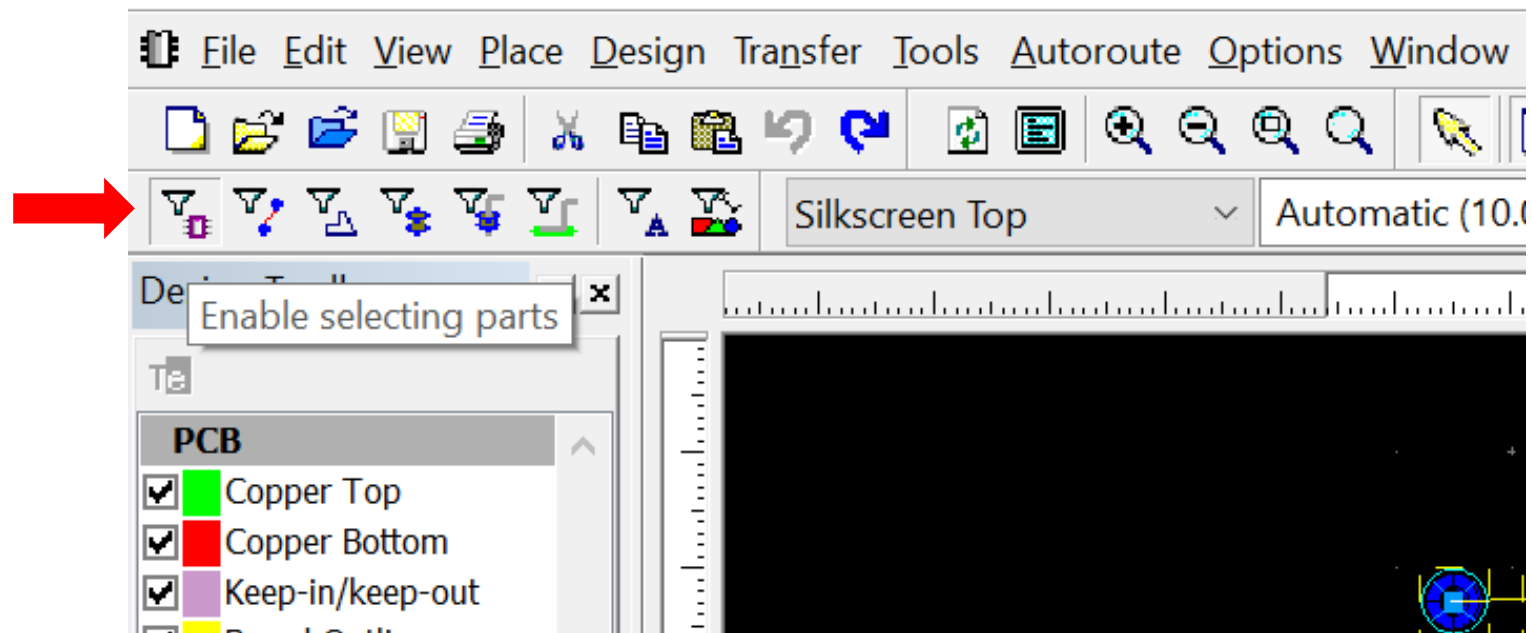
# Before you get started with the layout

- Right click on the border and select Properties (you might have to zoom in to do so)
- Make sure border width is 10 mil or so



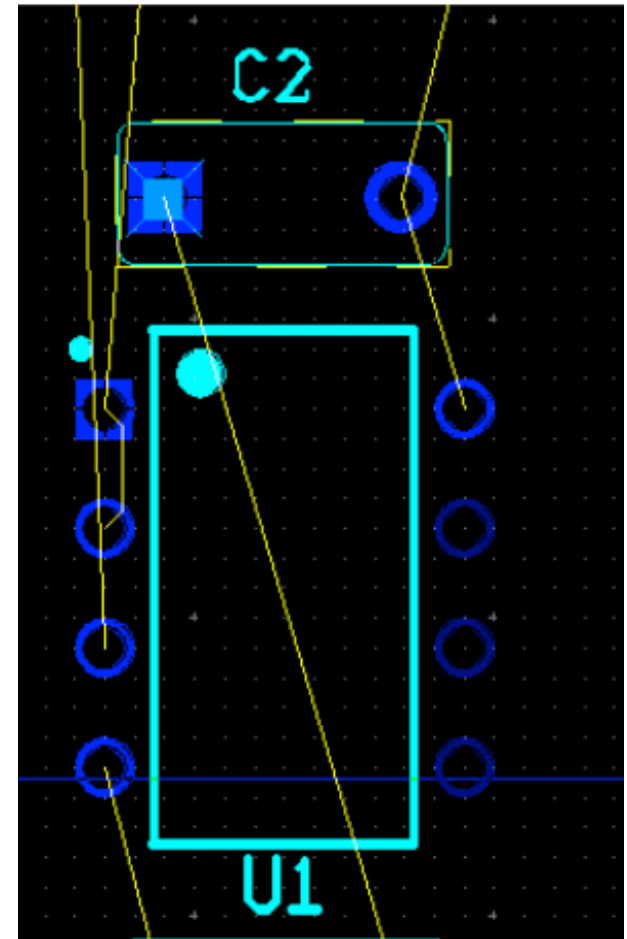
# Ultiboard

- Enable selecting parts, so you can move them
- Disable the rest of the selection tools, so you don't grab the wrong thing



# PCB Parts Layout

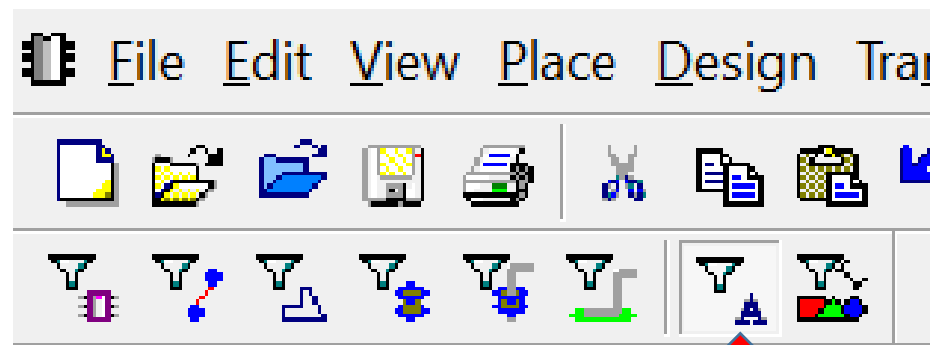
- Bypass caps should be as close as possible to the IC they are protecting to minimize stray inductance.
- Group parts by their function in the circuit to minimize trace lengths. Shorter traces means easier wire routing, less inductance, and less noise since a trace can act like an antenna.



Here bypass cap C2 is near the power pin (pin 8 in this case) of the IC it is shielding

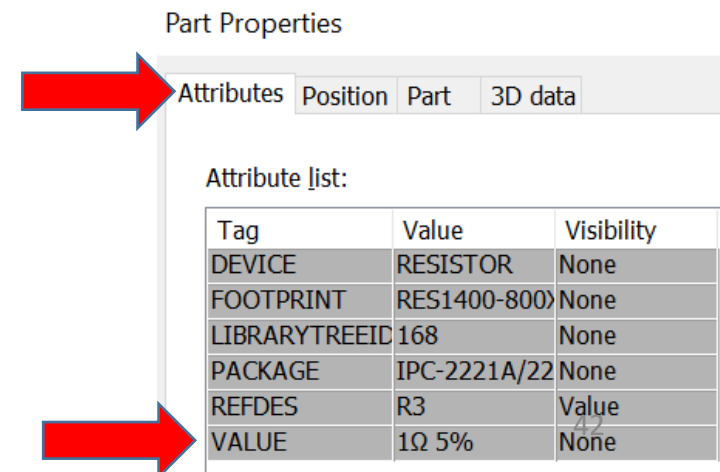
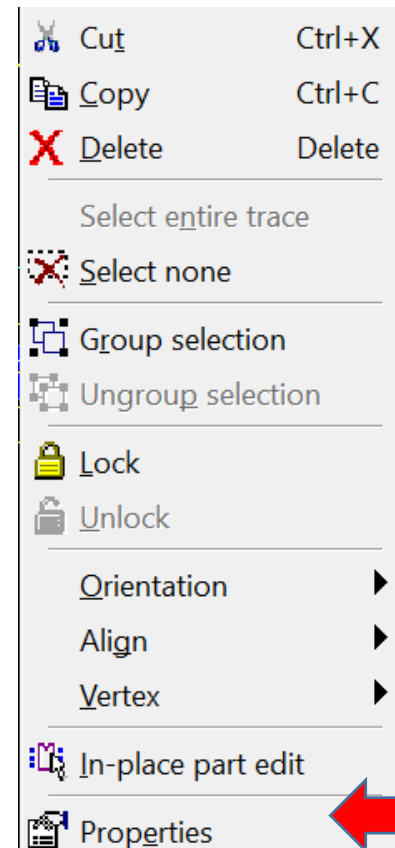
# Part Labels

- Use the Text Selection tool to move part labels
- Be sure labels are placed all in the same orientation so the board is easy to read
- Don't place labels under the part if you can avoid it
- It should be clear which part is associated with each label – don't crowd them or move them too far apart.
- Orientation of polarized parts and ICs should be clear.



# Part Labels

- Print component values on the board instead of (or in addition to) their net list reference – this allows anyone to populate the board with or without access to the original schematic.
- To have the values show up on the Silkscreen Top layer, right click on the component and select Properties.
- On the attributes tab, double-click on Value



# Part Labels

- Select Visible so that the label shows up.
- Set the Value to the component value
- For capacitors, just use the 3 digit cap code (e.g. 105 for a 1 $\mu$ F cap)
- For resistors, use a numerical value, but with R, K, or M instead of a decimal point which is hard to see.
  - 8.2 $\Omega$  => 8R2
  - 4.7K $\Omega$  => 4K7
  - 1.0M $\Omega$  => 1M0

The label for the value will probably need to be moved so it is close to the component with which it is associated

Attribute

Tag: VALUE

Value: 4K7

Visibility

☐ Invisible

☒ Value

☐ Value & tag

Alignment

☐ Top

☒ Center

☐ Bottom

☐ Left

☒ Center

☐ Right

Font

☒ Line:

☐ Thin

☐ Normal

☒ Bold

☐ Windows:

Font...

Height: 41.66665 mil

Rotation: 90.000000 °

Layer: Silkscreen Top

Color:  ☐ Mirror

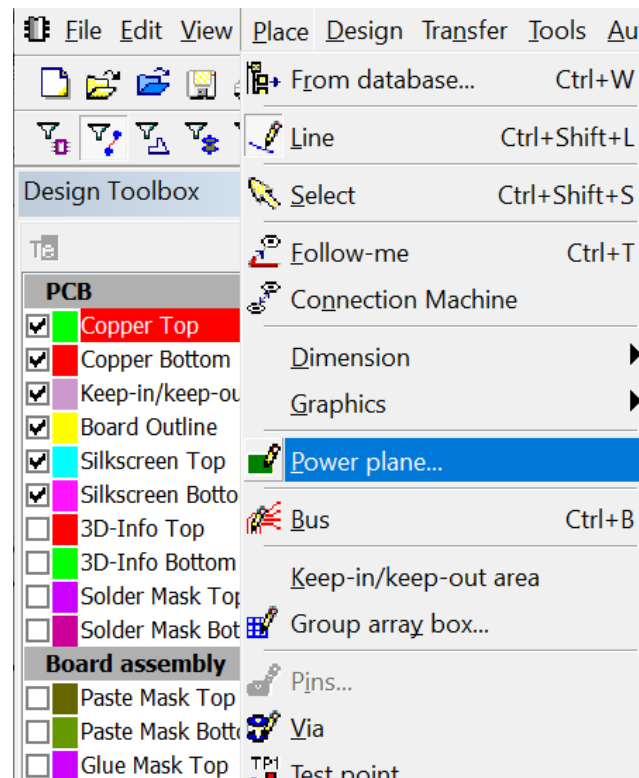
OK Cancel 43 Help



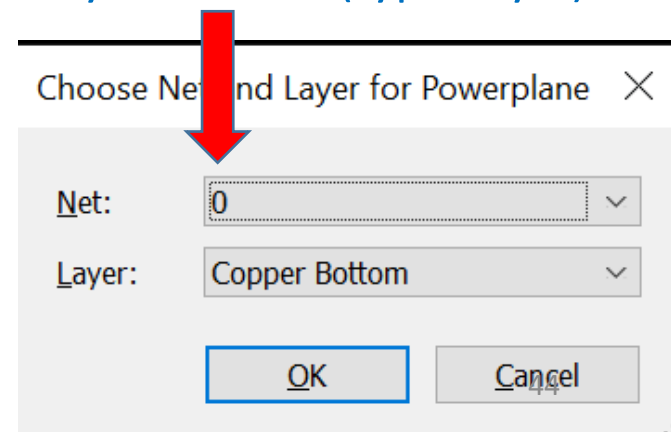
# Adding a Ground Plane

- A Ground Plane is a layer of copper across one side of the board that is used as the ground node.
- Ground Planes improve performance of most boards and make routing traces easier.

When not to use a ground plane: when you have so many traces on the bottom of the board that the ground plane gets sectioned into 'islands' which prevent easy current flow.

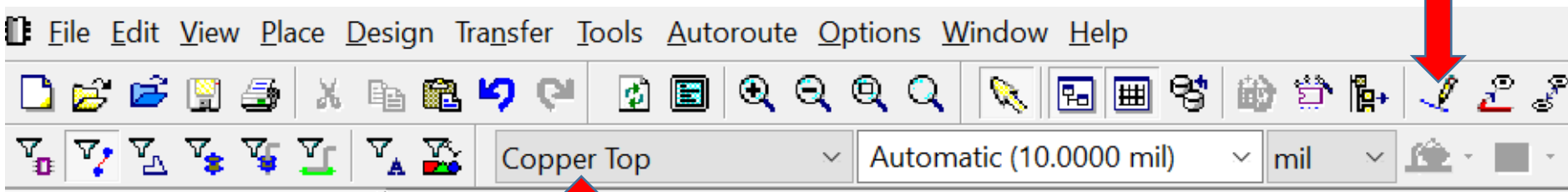


Set the Copper Bottom layer as your ground plane by linking it to the Net reference for ground in your circuit (typically 0)



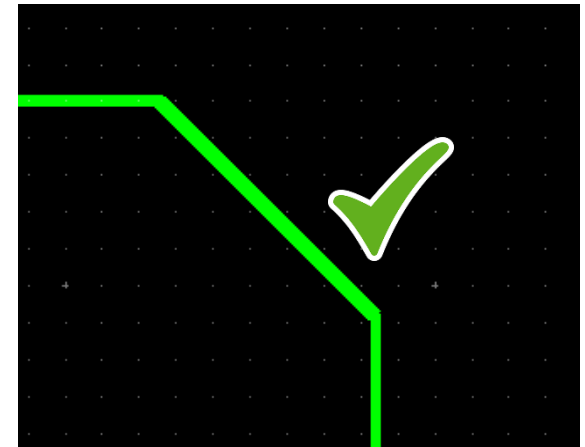
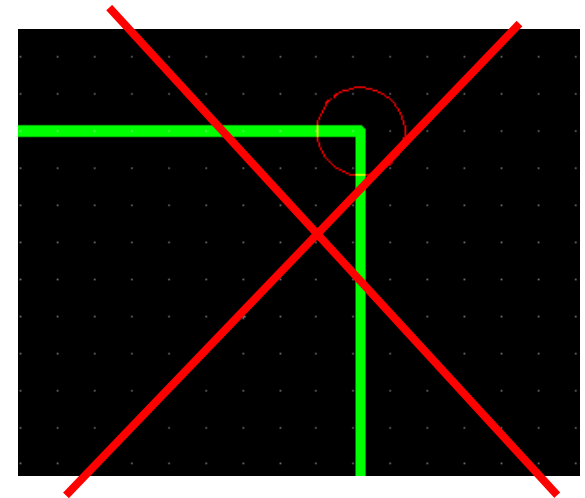
# Routing Traces

- Route the traces by first selecting the layer they will go on; start with Copper Top.
- Next select the Line Tool to draw them in.
- Traces carrying power are generally wider than signal traces; these are set for you in the template
- If you can't route two different traces without them crossing, route one on the Copper Top layer and the other on the Copper Bottom layer.
  - Ultiboard will automatically cut a path through the ground plane for anything on the bottom of the board.



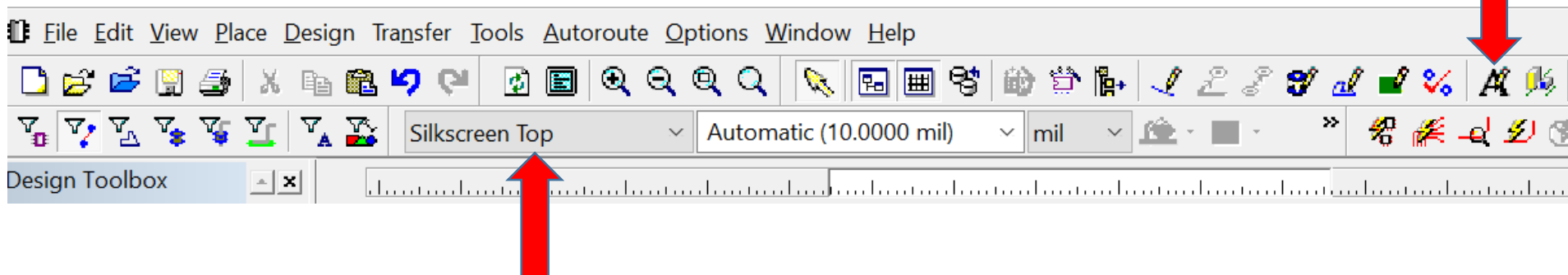
# Routing Traces: General Guidelines

- Don't use right angles when laying traces. The exceptions are at through-holes or T-junctions.
- Keep traces that cut through the ground plane to a minimum.
- Avoid running traces in parallel so they don't pick up noise from each other and create parasitic capacitance. The exception is clock traces since they have the same signal timing.
- Minimize the number of vias (holes in the board to go from top to bottom). They increase the cost of the board and add inductance to the trace.



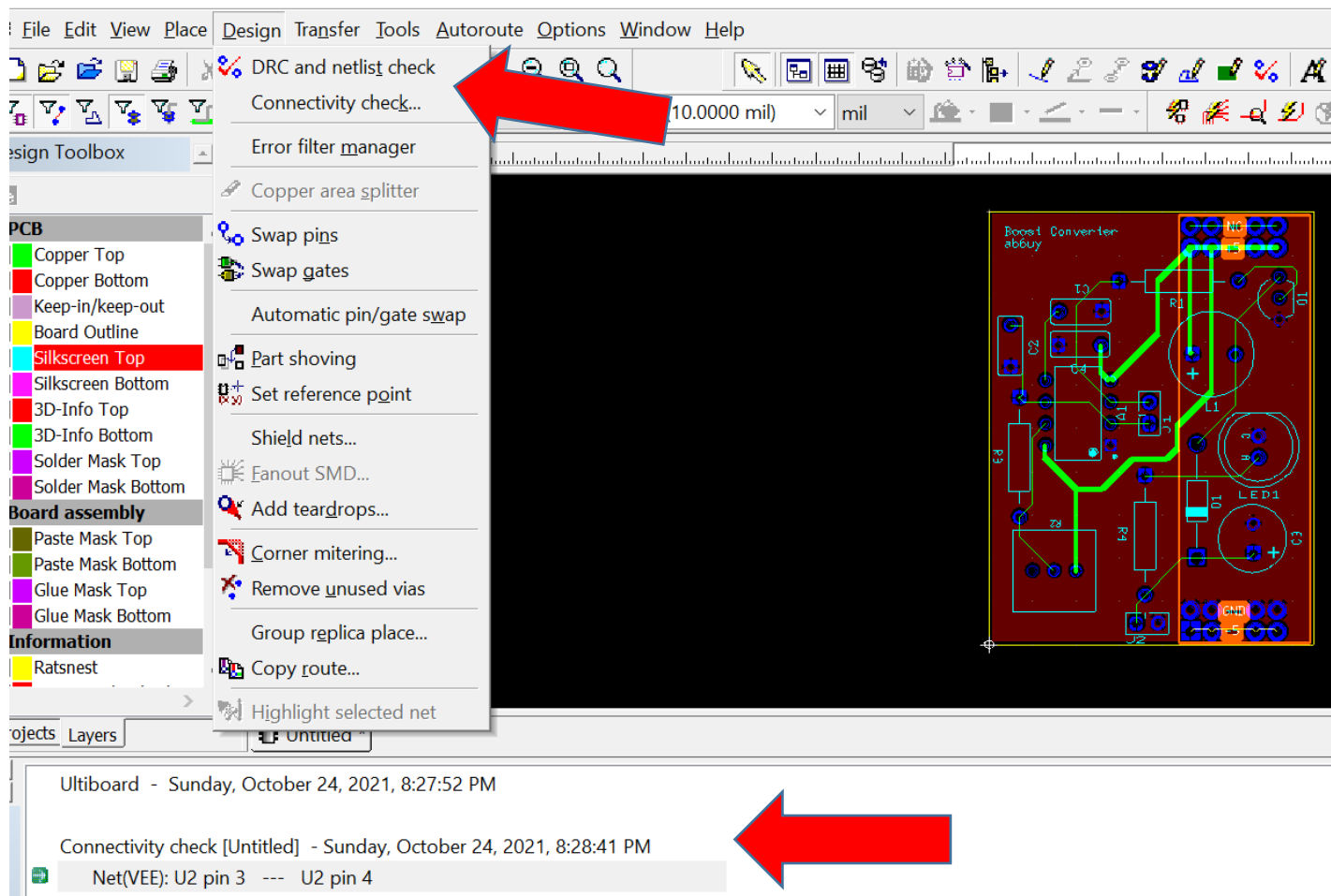
# Adding Notes

- Select Silkscreen Top Layer
- Use the Text tool to put notes/comments on your board
- Include Group Name, Date, and Class
- Make sure your traces were in a copper layer and not in the Silkscreen layer!



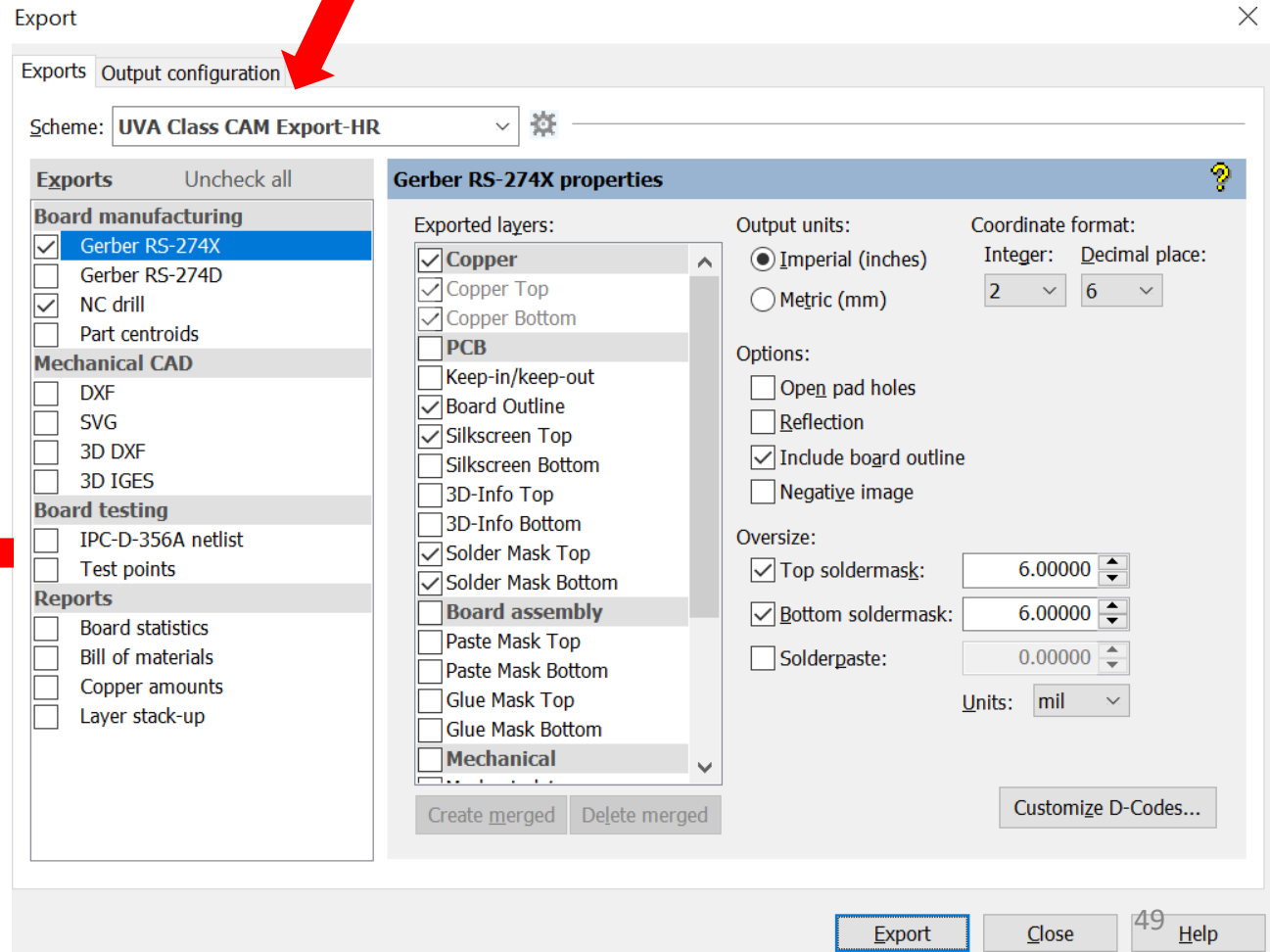
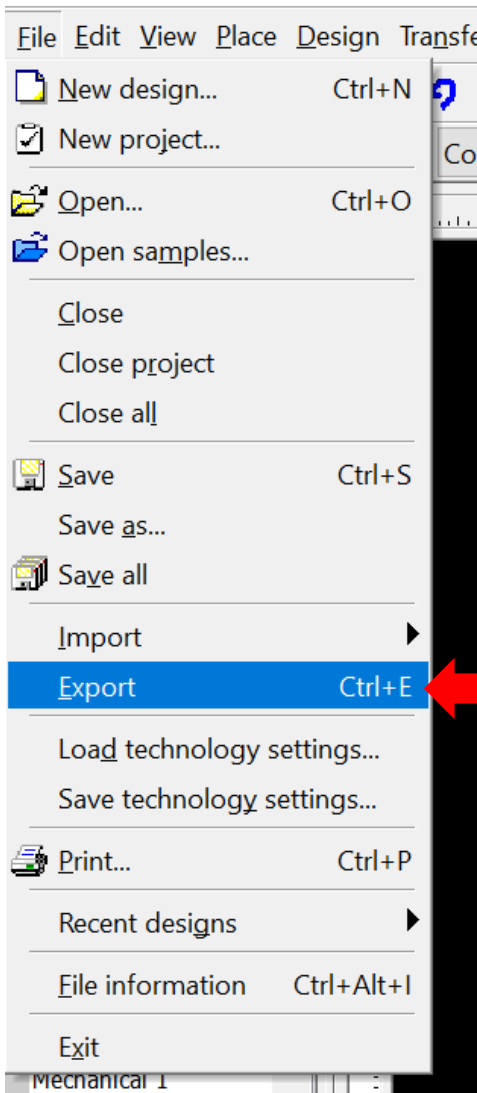
# Design Rule & Connectivity Checks

- Run the Design Rule Check (DRC) and Connectivity checks to catch basic routing errors or misconnections.
- Errors will display in the window at the bottom of the screen.



# Exporting Gerber Files

Download the UVA Class CAM Export file from Collab into your Multisim folder so it will appear here:



Export

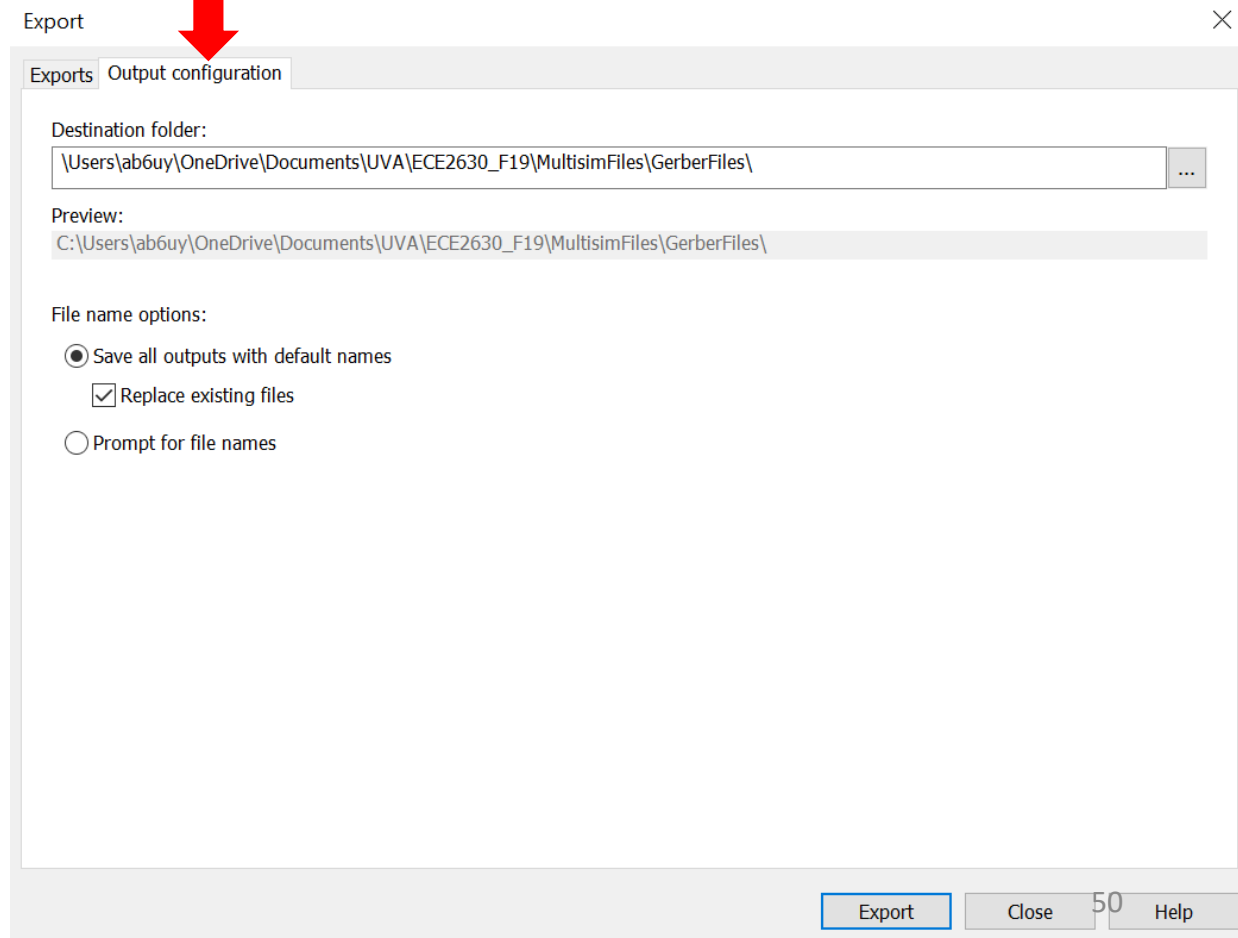
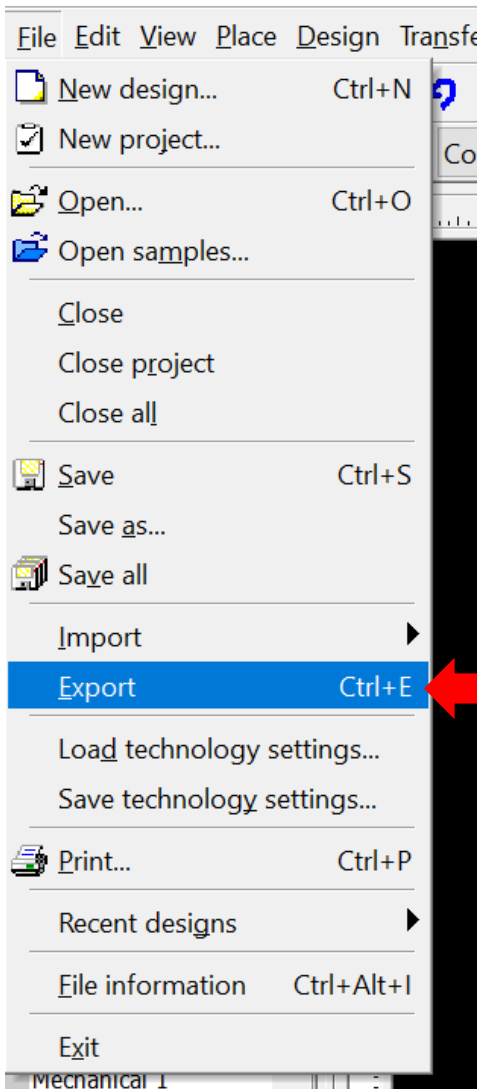
Close

49

Help

# Exporting Gerber Files

Choose a destination folder and Export the Gerber files



# Renaming Gerber Files

- Before the Gerber files can be checked using Design For Manufacturing (DFM) criteria, the Gerber files from Ultiboard need to be renamed, so as to conform to industry-standard naming conventions
- Download the **Rename Gerber Files** installer from Collab, and install it on your computer
- Then, use the DFM Submission document to submit the zip file produced by the **CamFileConverter** program to <http://freedfm.com>



# Design for Manufacturing (DFM)

## Design parameters:

- Set Part # & Revision
- Layer Count = 2
- Dimensions:
  - $X = 1.5$
  - $Y = 2.0$
- Soldermask on both sides
- Silkscreen on Top side
- No ITAR

**Please enter your contact information below:**

Company Name:	University of Virginia	Phone:	434-924-6108
First Name:	Adam	Last Name:	Barnes
Email 1:	ab6uy@virginia.edu		

**Please enter your quote specs and attributes below:**

Part #	ECE2630	Revision #	1	Layer Count	2
X Dimension	1.5	Y Dimension	2.0	Array	<input type="checkbox"/>
Array X Dim		Array Y Dim		Array Up	
Tab-Rout?	<input type="checkbox"/>	Scoring?	<input type="checkbox"/>		
Material Type	FR4	Finish Thickness	0.062"	Finish Plating	Lead Free Solder
				Gold Fingers	None
Soldermask Sides	Both Sides	Soldermask Color	Green	Copper Wt. (Outer)	1 oz
Silkscreen Sides	Top Side	Silkscreen Color	White	Copper Wt. (Inner)	None
Certifications & Qualifications:	IPC Class 2-A600	(Pricing Subject To File Review)			
	<input type="checkbox"/> AS9100?				
Vias:	Blind/Buried Vias?	None	Via-In-Pad?	None	
	Microvias?	None	(Finished hole size <= .006")		
	<input type="checkbox"/> Soldermask Plugged Vias?				
Additional Attributes:	<input type="checkbox"/> Controlled Dielectric?				
	<input type="checkbox"/> Controlled Impedance?	(Pricing Subject To File Review)			
	<input type="checkbox"/> Plated Slots?				
	<input type="checkbox"/> Plated Edges?	(Pricing Subject To File Review)			
	<input type="checkbox"/> Counterbores?	# Plated		# Non-Plated	
	<input type="checkbox"/> Countersinks?	# Plated		# Non-Plated	
	<input type="checkbox"/> Castellated Holes?	Min. Castellated Hole Size			
Quantities:	5	10	50	150	ITAR <input type="radio"/> Yes <input checked="" type="radio"/> No

# DFM Results

Receive 50 Dollars off your PCB order from FreeDFM.com! Promo Code: DFM50

Your Advanced Circuits quote number is: 4796675.

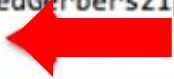
Click to view Quote and then click the link: FreeDFM Viewer 2.0 - to view the New Interactive FreeDFM Results for design TestTemplateFile1170707134514ZippedGerberszip:

<https://www.my4pcb.com/Net35/Login.aspx> Please note, accessing your quote has been modified. Clicking on the above link will take you to our login page. Please enter your user name and password and you will be able to retrieve your quote from the section -Existing PCB Quotes Without Orders-.

Click to view PLOTS for design TestTemplateFile1170707134514ZippedGerberszip:

<https://www.freedfm.com/freedfm/0025451604796675/results/plots.htm>

Click to view DFM results for design TestTemplateFile1170707134514ZippedGerberszip:

<https://www.freedfm.com/freedfm/0025451604796675/results/summary2.htm> 

Click here for a callback from our CAM department: <https://www.freedfm.com/callback.htm>

We need your feedback to improve. Click here for a quick survey: <https://www.freedfm.com/feedback.htm>

Multilayer pdf output results for design TestTemplateFile1170707134514ZippedGerberszip:

<https://www.freedfm.com/freedfm/0025451604796675/FreeDFM-v2.0/freeDFM.pdf>

Advanced Circuits FreeDFM

Your email from the freeDFM.com site will contain a link to your DFM results

# DFM Results



What FreeDFM found on your design

## Show Stoppers

We Found None!

## Problems Automatically Fixed

[Insufficient Soldermask Clearance \(6 violations\)](#)

[1](#) [2](#) [3](#) [4](#) [5](#)

[Insufficient Silkscreen Line Width \(248 violations\)](#)

[1](#) [2](#) [3](#) [4](#) [5](#)

# PCB Layout Submission

- This submission will consist of 3 files
  1. Your Ultiboard file (BoostConverter\_*yourComputingID*\_.ewprj)
  2. The zip file that contains the renamed Gerber files
  3. A file containing:
    - A screenshot showing the Electrical Rules Check passed in Multisim
    - A screenshot showing the Design Rules Check passed in Ultiboard
    - The results link in the email from [freedfm.com](https://freedfm.com)
    - A screenshot of the **No Showstoppers** page
- **This submission will be to Canvas and not Gradescope!**  
Gradescope only accepts pdfs so we will be using Canvas for this part of the project.
- Your full report will be submitted to Gradescope after you have populated the board and tested it.